

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD DATE
			2010-10-12

SCHEM, FLYING_DUTCHMAN, MLB, K91F
REV B RELEASE, 01/31/11

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65	5V / 3.3V Power Supply	K91_ERIC	10/08/2010
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67	CPU IMVP7 & AXG VCore Regulator	K91_ERIC	10/08/2010
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87	Graphics MUX (GMUX)	K91_MARY	08/03/2010
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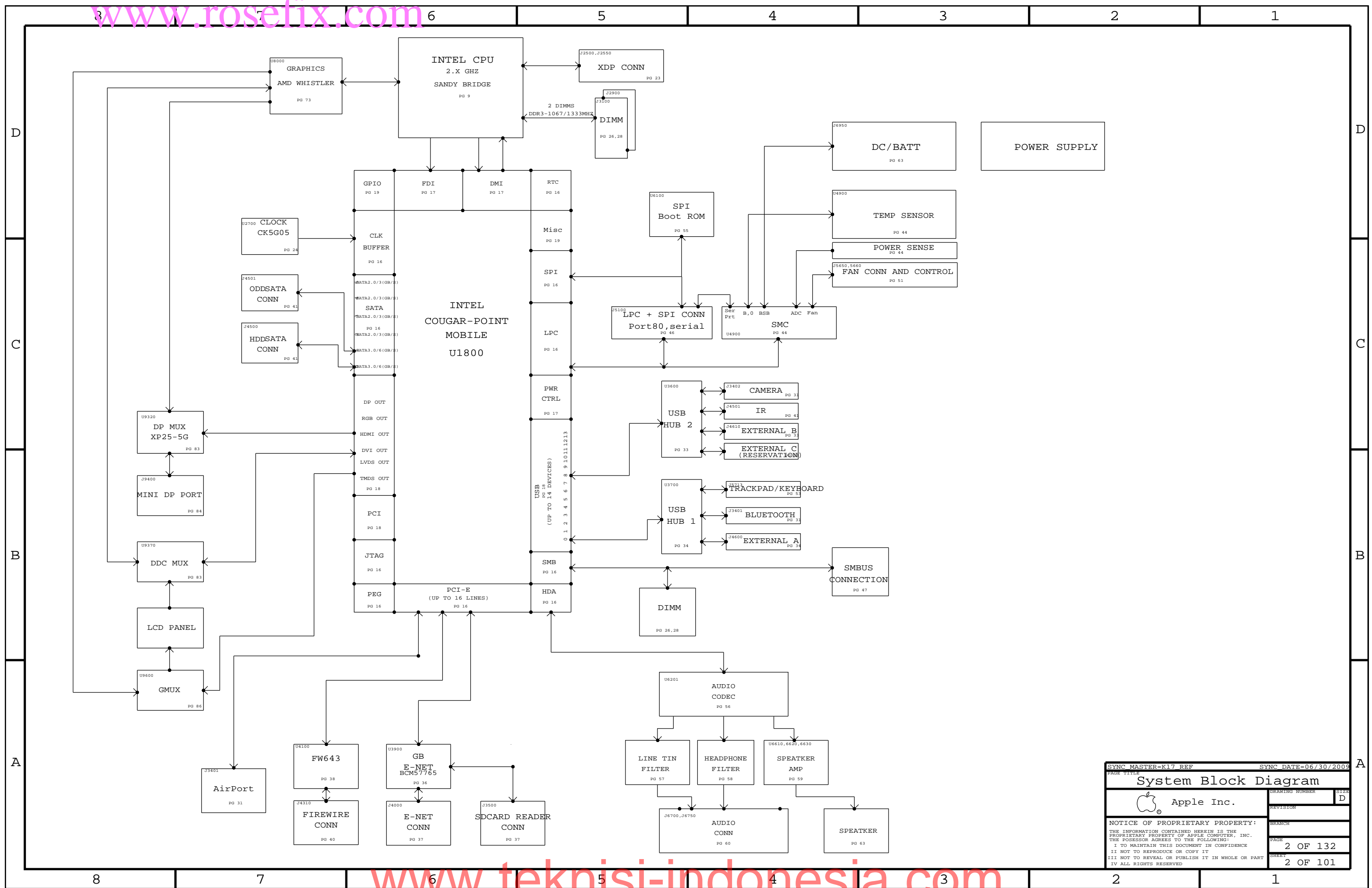
ALIASES RESOLVED

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-8620	1	SCHEM,MLB,K91	SCH	CRITICAL	
820-2915	1	PCBF,MLB,K91	PCB	CRITICAL	

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DRAWING TITLE		DRAWING NUMBER		SIZE	
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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
639-1468	PCBA,MLB,K91F,DG64	K91_COMMON,SODIMM:FOXCONN,CPU:2_2GHZ,GPU:WHISTLER,FB_1G_HYNIX,VRAM_DVP1,VRAM_DVP0,EEEE:DG64
639-1972	PCBA,MLB,K91F,DL83	K91_COMMON,SODIMM:HYBRID,CPU:2_2GHZ,GPU:WHISTLER,FB_1G_HYNIX,VRAM_DVP1,VRAM_DVP0,EEEE:DL83
639-1971	PCBA,MLB,K91F,DL82	K91_COMMON,SODIMM:MOLEX,CPU:2_2GHZ,GPU:WHISTLER,FB_1G_HYNIX,VRAM_DVP1,VRAM_DVP0,EEEE:DL82
639-1469	PCBA,MLB,K91F,DG65	K91_COMMON,SODIMM:FOXCONN,CPU:2_2GHZ,GPU:WHISTLER,FB_1G_SAMSUNG,VRAM_DVP0,EEEE:DG65
639-1970	PCBA,MLB,K91F,DL86	K91_COMMON,SODIMM:HYBRID,CPU:2_2GHZ,GPU:WHISTLER,FB_1G_SAMSUNG,VRAM_DVP0,EEEE:DL86
639-1956	PCBA,MLB,K91F,DL7W	K91_COMMON,SODIMM:MOLEX,CPU:2_2GHZ,GPU:WHISTLER,FB_1G_SAMSUNG,VRAM_DVP0,EEEE:DL7W
639-1470	PCBA,MLB,K91F,DG66	K91_COMMON,SODIMM:FOXCONN,CPU:2_3GHZ,GPU:WHISTLER,FB_1G_HYNIX,VRAM_DVP1,VRAM_DVP0,EEEE:DG66
639-1974	PCBA,MLB,K91F,DL87	K91_COMMON,SODIMM:HYBRID,CPU:2_3GHZ,GPU:WHISTLER,FB_1G_HYNIX,VRAM_DVP1,VRAM_DVP0,EEEE:DL87
639-1976	PCBA,MLB,K91F,DL88	K91_COMMON,SODIMM:MOLEX,CPU:2_3GHZ,GPU:WHISTLER,FB_1G_HYNIX,VRAM_DVP1,VRAM_DVP0,EEEE:DL88
639-1471	PCBA,MLB,K91F,DG67	K91_COMMON,SODIMM:FOXCONN,CPU:2_3GHZ,GPU:WHISTLER,FB_1G_SAMSUNG,VRAM_DVP0,EEEE:DG67
639-1973	PCBA,MLB,K91F,DL81	K91_COMMON,SODIMM:HYBRID,CPU:2_3GHZ,GPU:WHISTLER,FB_1G_SAMSUNG,VRAM_DVP0,EEEE:DL81
639-1954	PCBA,MLB,K91F,DL7T	K91_COMMON,SODIMM:MOLEX,CPU:2_3GHZ,GPU:WHISTLER,FB_1G_SAMSUNG,VRAM_DVP0,EEEE:DL7T
639-1573	PCBA,MLB,K91,DHMMV	K91_COMMON,SODIMM:FOXCONN,CPU:2_0GHZ,GPU:SEYMOUR,FB_256_HYNIX,EEEE:DHMMV
639-1945	PCBA,MLB,K91,DL7Q	K91_COMMON,SODIMM:HYBRID,CPU:2_0GHZ,GPU:SEYMOUR,FB_256_HYNIX,EEEE:DL7Q
639-1953	PCBA,MLB,K91,DL7R	K91_COMMON,SODIMM:MOLEX,CPU:2_0GHZ,GPU:SEYMOUR,FB_256_HYNIX,EEEE:DL7R
639-1574	PCBA,MLB,K91,DHMMW	K91_COMMON,SODIMM:FOXCONN,CPU:2_0GHZ,GPU:SEYMOUR,FB_256_SAMSUNG,EEEE:DHMMW
639-1959	PCBA,MLB,K91,DL80	K91_COMMON,SODIMM:HYBRID,CPU:2_0GHZ,GPU:SEYMOUR,FB_256_SAMSUNG,EEEE:DL80
639-1960	PCBA,MLB,K91,DL7Y	K91_COMMON,SODIMM:MOLEX,CPU:2_0GHZ,GPU:SEYMOUR,FB_256_SAMSUNG,EEEE:DL7Y
085-1901	K91/K91F DEVELOPMENT BOM	K91_DEVEL:ENG

K91 BOM GROUPS

BOM GROUP	BOM OPTIONS
K91_COMMON	ALTERNATE,COMMON,K91_COMMON1,K91_COMMON2,K91_PROGPARTS,K91_PROGPARTS1,UVGLUE_K91_K91F,K91_PVT
K91_COMMON1	CPUMEM_S0,SMC_DEBUG_YES,HUB1_2NONREM,HUB2_2NONREM,USBHUB_2513B
K91_COMMON2	GPUVID_1P11V,KB_BL,T29:YES,ENET_SD:B0,T29BST:Y,SDRV_PD,SDRV12C:MCU,T29_DP_HPD:ALL_OR
K91_PVT	BMON:PROD,VREFMRGN_NOT,XDP,XDP_CPU_BPM,BKLT:PROD,ISNS_ON:NO,LPCPLUS_R:YES
K91_PROGPARTS	GMUX_PROG,IR_PROG,TPAD_PROG:PVT,ENETROM_PROG:PVT,T29ROM:PROG,T29MCU:PROG
K91_PROGPARTS1	SMC_PROG:PVT,BOOTROM_PROG:PVT
K91_DEVEL:ENG	SNB_CPT_XDP,BMON:ENG,GMUX_TPAD_CONN,VREFMRGN,LPCPLUS_CONN:YES,LPCPLUS_R:YES,BKLT:ENG,SDV000_1SL,CPU1P11A_RNG,IMV1P1NS_RNG,ISNS_ON:YES,DEB00_ADC,DIG1_MIC
K91_DEVEL:PVT	SNB_CPT_XDP,LPCPLUS_CONN:YES,LPCPLUS_R:YES
SNB_CPT_XDP	XDP,XDP_CONN,XDP_CPU_BPM,XDP_PCH

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S4031	1	IC,CPU,SNB,S8030,PRQ,D2,2.0,45W,4+2,1.20,6M,BGA	U1000	CRITICAL	CPU:2_0GHZ
337S4032	1	IC,CPU,SNB,S8000,PRQ,D2,2.2,45W,4+2,1.30,6M,BGA	U1000	CRITICAL	CPU:2_2GHZ
337S4033	1	IC,CPU,SNB,S8000,PRQ,D2,2.3,45W,4+2,1.30,8M,BGA	U1000	CRITICAL	CPU:2_3GHZ
337S4029	1	IC,PCB,CODSARPOINT,SLA90,PRQ,B0928M65	U1800	CRITICAL	
337S3936	1	IC,GPU,AMD,WHISTLER,962PCBGA,40MM,ES	U8000	CRITICAL	GPU:WHISTLER
337S3979	1	IC,GPU,AMD,SEYMOUR,M2 LP,ES1,962BGA	U8000	CRITICAL	GPU:SEYMOUR
338S0945	1	IC,ASBP,LIGHTTRIDGE,S_LMAJ,PRQ,FCBGA,15X15MM	U3600	CRITICAL	T29:YES
343S0534	1	IC,ASIC,GBIT ETHERNET4SD CTRLR,686 QFN8X8,B0	U3900	CRITICAL	ENET_SD:B0
343S0494	1	IC,ASIC,GBIT ETHERNET4SD CTRLR,686 QFN8X8,A0	U3900	CRITICAL	ENET_SD:A0
338S0753	1	IC,PW643-E,1394B PHY/GHCI LNKX/PCI-E,12	U4100	CRITICAL	
333S0543	4	IC,SDRAM,GDDR5,32MX32,1.25GHz,E-DIE,HF	U8400,U8450,U8500,U8550	CRITICAL	FB_512_SAMSUNG
333S0564	4	IC,SDRAM,GDDR5,32MX32,1.25GHz,A-DIE1.35V	U8400,U8450,U8500,U8550	CRITICAL	FB_512_HYNIX
333S0571	4	IC,SDRAM,GDDR5,64MX32,3.6GBPS,C-DIE,HF	U8400,U8450,U8500,U8550	CRITICAL	FB_1G_SAMSUNG
333S0572	4	IC,SDRAM,GDDR5,64MX32,3.6GBPS,M-DIE,HF	U8400,U8450,U8500,U8550	CRITICAL	FB_1G_HYNIX
333S0543	2	IC,SDRAM,GDDR5,32MX32,1.25GHz,E-DIE,HF	U8500,U8550	CRITICAL	FB_256_SAMSUNG
333S0564	2	IC,SDRAM,GDDR5,32MX32,1.25GHz,A-DIE1.35V	U8500,U8550	CRITICAL	FB_256_HYNIX
353S3055	1	IC,P13VEDP212,X2 DISPLAYPORT 2+1 MUX,QFN	U9390	CRITICAL	
725-1479	1	MLB LOCITE UV EB CPU,PCH,T29,GPU,K91	UV_GLUE_K91_K91F	CRITICAL	UVGLUE_K91_K91F
516S0806	1	CONN,204P,SODIMM,SOCKET_DDR3,RAM,BGA,FOXCONN	J3100	CRITICAL	SODIMM:FOXCONN
516-0246	1	CONN,204P,SODIMM,SOCKET_DDR3,p=0.6M,FOXCONN	J2900	CRITICAL	SODIMM:FOXCONN
516S0805	1	CONN,204P,SODIMM,SOCKET_DDR3,RAM,BGA,MOLEX	J3100	CRITICAL	SODIMM:MOLEX
516-0245	1	CONN,204P,SODIMM,SOCKET_DDR3,p=0.6M,MOLEX	J2900	CRITICAL	SODIMM:MOLEX
516S0805	1	CONN,204P,SODIMM,SOCKET_DDR3,RAM,BGA,MOLEX	J3100	CRITICAL	SODIMM:HYBRID
516-0246	1	CONN,204P,SODIMM,SOCKET_DDR3,p=0.6M,FOXCONN	J2900	CRITICAL	SODIMM:HYBRID

ETHERNET ROM

335S0663	1	IC,FLASH,SERIAL,SP1,1MBIT,DVT,8P,SOIC	U3990	CRITICAL	ENETROM_BLANK
341S2685	1	IC,ENET,1MBITFLASH,CIV REV01,K74/K75,K40	U3990	CRITICAL	ENETROM_PROG:A0_SD
341S2973	1	IC,ENET,1MBITFLASH,CIV REV01,K60/K62	U3990	CRITICAL	ENETROM_PROG:B0_SD
341S3026	1	IC,ENET,1MBITFLASH,CIV REV01,K901/K91/K92	U3990	CRITICAL	ENETROM_PROG:EVT
341S3096	1	IC,ENET ROM,1MBIT,DVT,PVT,K901/K91x	U3990	CRITICAL	ENETROM_PROG:PVT

Bar Code Labels / EEEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DDKG]	CRITICAL	EEEE:DDKG
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG63]	CRITICAL	EEEE:DG63
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG64]	CRITICAL	EEEE:DG64
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG65]	CRITICAL	EEEE:DG65
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG66]	CRITICAL	EEEE:DG66
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG67]	CRITICAL	EEEE:DG67
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DHMV]	CRITICAL	EEEE:DHMV
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DHMM]	CRITICAL	EEEE:DHMM
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL81]	CRITICAL	EEEE:DL81
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL82]	CRITICAL	EEEE:DL82
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL83]	CRITICAL	EEEE:DL83
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL84]	CRITICAL	EEEE:DL84
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL85]	CRITICAL	EEEE:DL85
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL86]	CRITICAL	EEEE:DL86
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL87]	CRITICAL	EEEE:DL87
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL88]	CRITICAL	EEEE:DL88
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL89]	CRITICAL	EEEE:DL89
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL7Q]	CRITICAL	EEEE:DL7Q
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL7R]	CRITICAL	EEEE:DL7R
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL7T]	CRITICAL	EEEE:DL7T
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL7V]	CRITICAL	EEEE:DL7V
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL7W]	CRITICAL	EEEE:DL7W
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL7Y]	CRITICAL	EEEE:DL7Y
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL80]	CRITICAL	EEEE:DL80

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
157S0058	157S0055		ALL	Delta alt to TDK Magnetics
152S0896	152S0518		ALL	MAG LAYERS ALT TO CYNTEC
155S0457	155S0329		ALL	MAG LAYERS ALT TO MURATA
353S2805	353S2603		ALL	Fairchild wafer option
128S0264	128S0257		ALL	Sanyo alt to Kemet
128S0303	128S0282		ALL	Panasonic alt to Sanyo
353S3085	353S1658		ALL	ST Micro alt to LT
376S0972	376S0612		ALL	ROHM alt to Toshiba N-FET
376S0855	376S0613		ALL	Diodes alt to Toshiba dual N-FET
138S0676	138S0691		ALL	Murata alt to Samsung cap
138S0652	138S0648		ALL	Samsung / Murata alt for Tokyo Tachen
138S0681	138S0638		ALL	Tokyo Tachen alt for Samsung
152S0685	152S0796		ALL	Intel/WinChip/DSP alt for Cypress
376S0977	376S0859		ALL	ROHM alt for Rohm
353S2592	353S3199		ALL	Intel/Altera/Altera alt for Samsung/WinChip alt
335S0550	335S0777		ALL	add 4K Byte aa alternative to 3K
371S0679	371S0652		ALL	RSP alternative for pin diodes
138S0671	138S0673		ALL	Tokyo Tachen alt for Murata 10 uf caps

Programmables - All Builds

341S2830	1	IC,CPLD,LATTICE,GMUX,K91/K91F	U9600	CRITICAL	GMUX_PROG
336S0042	1	IC,PLD,LATTICE,LPX92-SK-5,132 BALL CHBGA	U9600	CRITICAL	GMUX_BLANK
341S2384	1	IR,ENCORE II,C70638333-IFAC	U4800	CRITICAL	IR_PROG
341S3129	1	IC,T29 EEPROM,PVT,K9x	U3690	CRITICAL	T29ROM:PROG
335S0777	1	IC,EEPROM,SERIAL,8KB,SOIC	U3690	CRITICAL	T29ROM:BLANK
341S3128	1	IC,PROGRAMM,LPCL112A,T29 PORT MCU,PVT,HVQFN25	U9330	CRITICAL	T29MCU:PROG
337S3997	1	IC,MCU,32B,LPCL112A,16KB/25B,HVQFN25	U9330	CRITICAL	T29MCU:BLANK
341S2957	1	IC,GPU ROM,K91/F,K92,PROG	U8701	CRITICAL	GPUROM:PROG
335S0724	1	IC,GPU ROM,K91/F,K92,BLANK	U8701	CRITICAL	GPUROM:BLANK

SMC

338S0895	1	IC,SMC,RSB/2117,59KX5MM,TLP	U4900	CRITICAL	SMC_BLANK
341S2854	1	IC,SMC,DEVELOPMENT-PROTO0,K91	U4900	CRITICAL	SMC_PROG:PROTO0
341S2935	1	IC,SMC,DEVELOPMENT-PROTO1,K91	U4900	CRITICAL	SMC_PROG:PROTO1
341S2994	1	IC,SMC,DEVELOPMENT-PROTO2,K91	U4900	CRITICAL	SMC_PROG:PROTO2
341S2861	1	IC,SMC,DEVELOPMENT-EVT,K91	U4900	CRITICAL	SMC_PROG:EVT
341S2864	1	IC,SMC,DEVELOPMENT-DVT,K91	U4900	CRITICAL	SMC_PROG:DVT
341S2867	1	IC,SMC,DEVELOPMENT-PVT,K91	U4900	CRITICAL	SMC_PROG:PVT

EFI ROM

335S0740	1	64 MBIT SPI SERIAL DUAL I/O FLASH	U6100	CRITICAL	BOOTROM_BLANK
341S2893	1	IC,EFI,ROM,PROTO0, K90/K901/K91/K91F/K92	U6100	CRITICAL	BOOTROM_PROG:PROTO0
341S2934	1	IC,EFI,ROM,PROTO1, K90/K901/K91/K91F/K92	U6100	CRITICAL	BOOTROM_PROG:PROTO1
341S2991	1	IC,EFI,ROM,PROTO2, K90/K901/K91/K91F/K92	U6100	CRITICAL	BOOTROM_PROG:PROTO2
341S2894	1	IC,EFI,ROM,EVT, K90/K901/K91/K91F/K92	U6100	CRITICAL	BOOTROM_PROG:EVT
341S2895	1	IC,EFI,ROM,DVT, K90/K901/K91/K91F/K92	U6100	CRITICAL	BOOTROM_PROG:DVT
341S2896	1	IC,EFI,ROM,PVT, K90/K901/K91/K91F/K92	U6100	CRITICAL	BOOTROM_PROG:PVT

PSOC


341S2902	1	IC,TP PSOC,K9x,PROTO0	U5701	CRITICAL	TPAD_PROG:PROTO0
341S2940	1	IC,TP PSOC,K9x,PROTO1	U5701	CRITICAL	TPAD_PROG:PROTO1
341S3001	1	IC,TP PSOC,K9x,PROTO2	U5701	CRITICAL	TPAD_PROG:PROTO2
341S3024	1	IC,TP PSOC,K9x,EVT	U5701	CRITICAL	TPAD_PROG:EVT
341S3099	1	IC,TP PSOC,K9x,DVT,PVT	U5701	CRITICAL	TPAD_PROG:PVT

SYNC MASTER=K17 REF

SYNC DATE=05/28/2009

PAGE TITLE

BOM Configuration

 Apple Inc.

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SHEET

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Functional Test Points

J5650 (LEFT FAN CONN)		USB PORTS	
FUNC_TEST	PP5V S0	TRUE PP5V S3 RTUSB A F	42
TRUE	FAN LT PWM	TRUE USB2 LT1 N	42 98
TRUE	FAN LT TACH	TRUE USB2 LT1 P	42 98
J5660 (RIGHT FAN CONN)		GND	
TRUE	PP5V S0	TRUE PP5V S3 RTUSB B F	42
TRUE	FAN RT PWM	TRUE USB LT2 N	42 98
TRUE	FAN RT TACH	TRUE USB LT2 P	42 98
TRUE	GND	TRUE	GND
J6780 (MIC CONN)		GND	
TRUE	BI MIC N	TRUE	GND
TRUE	BI MIC SHIELD	TRUE	GND
TRUE	BI MIC P	TRUE	GND
J3401 & J3402 (AIRPORT/BT/CAMERA CONN)		GND	
TRUE	PCIE AP D2R P	TRUE	GND
TRUE	PCIE AP D2R N	TRUE	GND
TRUE	PCIE AP R2D P	TRUE	GND
TRUE	PCIE AP R2D N	TRUE	GND
TRUE	PCIE CLK100M AP CONN P	TRUE	GND
TRUE	PCIE CLK100M AP CONN N	TRUE	GND
TRUE	AP CLKREQ O L	TRUE	GND
TRUE	PCIE WAKE L	TRUE	GND
TRUE	WIFI EVENT L	TRUE	GND
TRUE	AP RESET CONN L	TRUE	GND
TRUE	PP3V3 WLAN	TRUE	GND
TRUE	PP5V S3 ALSCAMERA F	TRUE	GND
TRUE	SMBUS SMC A S3 SDA	TRUE	GND
TRUE	USB CAMERA CONN P	TRUE	GND
TRUE	USB CAMERA CONN N	TRUE	GND
TRUE	CONN USB2 BT P	TRUE	GND
TRUE	CONN USB2 BT N	TRUE	GND
TRUE	SMBUS SMC 0 S0 SCL	TRUE	GND
TRUE	SMBUS SMC 0 S0 SDA	TRUE	GND
J6781 & J6782 (SPEAKERS CONN)		GND	
TRUE	SPKRCONN L OUT P	TRUE	GND
TRUE	SPKRCONN L OUT N	TRUE	GND
TRUE	SPKRCONN R OUT P	TRUE	GND
TRUE	SPKRCONN R OUT N	TRUE	GND
TRUE	SPKRCONN S OUT P	TRUE	GND
TRUE	SPKRCONN S OUT N	TRUE	GND
J9000 (LVDS CONN)		GND	
TRUE	PP3V3 SW LCD	TRUE	GND
TRUE	PP3V3 S0	TRUE	GND
TRUE	PPVOUT S0 LCDBKLT	TRUE	GND
TRUE	LVDS DDC CLK	TRUE	GND
TRUE	LVDS DDC DATA	TRUE	GND
TRUE	LVDS CONN A DATA P<0>	TRUE	GND
TRUE	LVDS CONN A DATA N<0>	TRUE	GND
TRUE	LVDS CONN A DATA P<1>	TRUE	GND
TRUE	LVDS CONN A DATA N<1>	TRUE	GND
TRUE	LVDS CONN A DATA P<2>	TRUE	GND
TRUE	LVDS CONN A DATA N<2>	TRUE	GND
TRUE	LVDS CONN A CLK F P	TRUE	GND
TRUE	LVDS CONN A CLK F N	TRUE	GND
TRUE	LVDS CONN B DATA P<0>	TRUE	GND
TRUE	LVDS CONN B DATA N<0>	TRUE	GND
TRUE	LVDS CONN B DATA P<1>	TRUE	GND
TRUE	LVDS CONN B DATA N<1>	TRUE	GND
TRUE	LVDS CONN B DATA P<2>	TRUE	GND
TRUE	LVDS CONN B DATA N<2>	TRUE	GND
TRUE	LVDS CONN B CLK F P	TRUE	GND
TRUE	LVDS CONN B CLK F N	TRUE	GND
TRUE	LED RETURN 1	TRUE	GND
TRUE	LED RETURN 2	TRUE	GND
TRUE	LED RETURN 3	TRUE	GND
TRUE	LED RETURN 4	TRUE	GND
TRUE	LED RETURN 5	TRUE	GND
TRUE	LED RETURN 6	TRUE	GND
J5800 (IPD FLEX CONN)		GND	
TRUE	PP18V5 S4	TRUE	GND
TRUE	Z2 HOST INTN	TRUE	GND
TRUE	Z2 MOSI	TRUE	GND
TRUE	Z2 CS L	TRUE	GND
TRUE	Z2 SCL	TRUE	GND
TRUE	Z2 DEBUG3	TRUE	GND
TRUE	Z2 MISO	TRUE	GND
TRUE	Z2 BOOST EN	TRUE	GND
TRUE	Z2 SCL	TRUE	GND
TRUE	Z2 CLIN	TRUE	GND
TRUE	PP3V3 S5	TRUE	GND
TRUE	PP3V3 S5 AVREF	TRUE	GND
TRUE	PP3V42 G3H	TRUE	GND
TRUE	PP5V S0	TRUE	GND
TRUE	PP5V S3	TRUE	GND
TRUE	PP5V S5	TRUE	GND
TRUE	PPBUS G3H	TRUE	GND
TRUE	PPDCIN G3H	TRUE	GND
TRUE	PPVCORE GPU	TRUE	GND
TRUE	PPVCORE S0 CPU	TRUE	GND
TRUE	PPVCORE S0 GFX	TRUE	GND
TRUE	PPVP FW	TRUE	GND
TRUE	PPVTIDDR S3	TRUE	GND
J6900 (DC POWER CONN)		GND	
TRUE	ADAPTER SENSE	TRUE	GND
TRUE	PP18V5 DCIN FUSE	TRUE	GND
J4501 (SATA HDD CONN)		GND	
TRUE	PP5V S0 HDD PLT	TRUE	GND
TRUE	SATA HDD R2D P	TRUE	GND
TRUE	SATA HDD R2D N	TRUE	GND
TRUE	SATA HDD D2R C N	TRUE	GND
TRUE	SATA HDD D2R C P	TRUE	GND
J5815 (KBD BACKLIGHT CONN)		GND	
TRUE	KBDLED ANODE	TRUE	GND
TRUE	SMC KBDLED PRESENT L	TRUE	GND
J6995 (BAT LED CONN)		GND	
TRUE	PP3V42 G3H	TRUE	GND
TRUE	SMBUS SMC BSA SDA	TRUE	GND
TRUE	SMBUS SMC BSA SCL	TRUE	GND
TRUE	NC SMC BS ALRT L	TRUE	GND
J6950 (MAIN BATT CONN)		GND	
TRUE	PPVBAT G3H CONN	TRUE	GND
TRUE	SMBUS SMC BSA SCL	TRUE	GND
TRUE	SMBUS SMC BSA SDA	TRUE	GND
TRUE	NC SMC BS ALRT L	TRUE	GND
J54501 (SATA HDD CONN)		GND	
TRUE	PP5V S0 HDD PLT	TRUE	GND
TRUE	SATA HDD R2D P	TRUE	GND
TRUE	SATA HDD R2D N	TRUE	GND
TRUE	SATA HDD D2R C N	TRUE	GND
TRUE	SATA HDD D2R C P	TRUE	GND
J5815 (KBD BACKLIGHT CONN)		GND	
TRUE	KBDLED ANODE	TRUE	GND
TRUE	SMC KBDLED PRESENT L	TRUE	GND
J6995 (BAT LED CONN)		GND	
TRUE	PP3V42 G3H	TRUE	GND
TRUE	SMBUS SMC BSA SDA	TRUE	GND
TRUE	SMBUS SMC BSA SCL	TRUE	GND
TRUE	NC SMC BS ALRT L	TRUE	GND
J6950 (MAIN BATT CONN)		GND	
TRUE	PPVBAT G3H CONN	TRUE	GND
TRUE	SMBUS SMC BSA SCL	TRUE	GND
TRUE	SMBUS SMC BSA SDA	TRUE	GND
TRUE	NC SMC BS ALRT L	TRUE	GND

J5713 (KEY BOARD CONN)

TRUE	PP3V3 S3	42
TRUE	PP3V42 G3H	42
TRUE	WS KBD1	52
TRUE	WS KBD2	52
TRUE	WS KBD3	52
TRUE	WS KBD4	52
TRUE	WS KBD5	52
TRUE	WS KBD6	52
TRUE	WS KBD7	52
TRUE	WS KBD8	52
TRUE	WS KBD9	52
TRUE	WS KBD10	52
TRUE	WS KBD11	52
TRUE	WS KBD12	52
TRUE	WS KBD13	52
TRUE	WS KBD14	52
TRUE	WS KBD15 CAP	52
TRUE	WS KBD16 NUM	52
TRUE	WS KBD17	52
TRUE	WS KBD18	52
TRUE	WS KBD19	52
TRUE	WS KBD20	52
TRUE	WS KBD21	52
TRUE	WS KBD22	52
TRUE	WS KBD23	52
TRUE	WS KBD ONOFF L	52
TRUE	WS LEFT SHIFT KBD	52
TRUE	WS LEFT OPTION KBD	52
TRUE	WS CONTROL KBD	52

FUNC_TEST

TRUE	BKLT EN	42
TRUE	TP ISSP SCLK P1_1	52
TRUE	TP ISSP SDATA P1_0	52
TRUE	LCD BKLT PWM	87
TRUE	LPCPLUS GPIO	19
TRUE	LPCPLUS RESET L	25
TRUE	LPC AD<0..3>	46
TRUE	LPC_CLK33M LPCPLUS	25
TRUE	LPC_FRAME L	16
TRUE	LPC PWRDWN L	17
TRUE	LPC SERIO	16
TRUE	PM CLKRUN L	17
TRUE	PM SYSRST L	17
TRUE	SMC MD1	44
TRUE	SMC NMI	44
TRUE	SMC ONOFF L	44
TRUE	SMC RESET L	44
TRUE	SMC RX L	44
TRUE	SMC TCK	44
TRUE	SMC TDI	44
TRUE	SMC TDO	44
TRUE	SMC TMS	44
TRUE	SMC TRST L	44
TRUE	SMC TX L	44
TRUE	SPIROM USE MLB	19
TRUE	SPI ALT CLK	46
TRUE	SPI ALT CS L	46
TRUE	SPI ALT MISO	46
TRUE	SPI ALT MOSI	46
TRUE	SYS LED ANODE R	41

NO_TEST=TRUE

TRUE	T29 D2R P<1..0>	33
TRUE	T29 D2R N<1..0>	33
TRUE	T29 D2R C P<1..0>	33
TRUE	T29 D2R C N<1..0>	33
TRUE	T29 R2D C P<1..0>	33
TRUE	T29 R2D C N<1..0>	33
TRUE	T29 R2D P<1..0>	33
TRUE	T29 R2D N<1..0>	33
TRUE	T29DPA ML P<3..0>	84
TRUE	T29DPA ML N<3..0>	84
TRUE	DP T29SNK0 AUXCH C_N	33
TRUE	DP T29SNK0 AUXCH P	33
TRUE	DP T29SNK0 AUXCH N	33
TRUE	DP T29SNK0 ML C P<3..0>	33
TRUE	DP T29SNK0 ML C N<3..0>	33
TRUE	DP T29SNK0 ML P<3..0>	33
TRUE	DP T29SNK0 ML N<3..0>	33
TRUE	DP T29SNK1 AUXCH C_P	33
TRUE	DP T29SNK1 AUXCH C_N	33
TRUE	DP T29SNK1 AUXCH P	33
TRUE	DP T29SNK1 AUXCH N	33
TRUE	DP T29SNK1 ML C P<3..0>	33
TRUE	DP T29SNK1 ML C N<3..0>	33
TRUE	DP T29SNK1 ML P<3..0>	33
TRUE	DP T29SNK1 ML N<3..0>	33
TRUE	DP T29SRC AUXCH CN	33
TRUE	DP T29SRC ML C P<3..0>	33
TRUE	DP T29SRC ML C N<3..0>	33
TRUE	DP SDRVA ML C P<0..0>	84
TRUE	DP SDRVA ML C N<0..0>	84
TRUE	DP SDRVA ML P<2..0>	84
TRUE	DP SDRVA ML N<2..0>	84
TRUE	TP T29 PCIE RESET L	33
TRUE	TP T29 PCIE RESET L	33
TRUE	TP T29 PCIE RESET L	33
TRUE	TP T29 PCIE RESET L	33
TRUE	T29DPA D2R1 AUXCH N	85
TRUE	T29DPA D2R1 AUXCH P	85
TRUE	T29 D2R1 BIAS	85

NC NO TESTS

TRUE	TP FW643 NAND TREE	38
TRUE	TP FW643 OCR10 CTL	38
TRUE	TP FW643 SCIFCLK	38
TRUE	TP FW643 SCIFDRAIN	38
TRUE	TP FW643 SCIFDOUT	38
TRUE	TP FW643 SCIFMC	38
TRUE	TP SMC P10	44
TRUE	TP FW643 SDA	38
TRUE	TP FW643 SE	38
TRUE	TP FW643 SM	38
TRUE	TP FW643 CE	38
TRUE	TP FW643 FW620 L	38
TRUE	TP FW643 JASI EN	38
TRUE	DMI S2N N<1>	37
TRUE	DMI S2N P<1>	37
TRUE	FDI DATA N<1>	90
TRUE	FDI DATA P<1>	90
TRUE	FDI FSYNCL<1..0>	90
TRUE	FDI LSYNCL<1..0>	90
TRUE	FDI INT	90

TRUE	TP FW643 VAUX ENABLE	38
TRUE	TP FW643 VBUP	38
TRUE	TP FW643 TCK	38
TRUE	TP FW643 TDO	38
TRUE	TP FW643 TMS	38
TRUE	TP FW643 SMC P10	44
TRUE	TP P7 7	52
TRUE	TP SMC SCL	52
TRUE	TP SMC P24	52
TRUE	TP SMC SDA	52
TRUE	TP PSOC SCL	52
TRUE	TP PSOC SDA	52
TRUE	TP DC TEST BH1 BG2	12
TRUE	TP DC TEST BH3 BJ2	12
TRUE	TP USB HUB1 OCS1	24
TRUE	TP USB HUB1 PRTWR1	24
TRUE	TP USB HUB2 OCS1	24
TRUE	TP USB HUB2 PRTWR1	24
TRUE	TP DC TEST A62	12
TRUE	TP DC TEST D65	12
TRUE	TP SMC PF5	44

ICT Test Points

CPU NO_TESTS

NO_TEST	TP CPU RSVD<65..62>	TRUE	NC TP CPU RSVD<65..62>
TRUE	TP CPU RSVD<58..45>	TRUE	NC TP CPU RSVD<58..45>
TRUE	TP CPU RSVD<43..32>	TRUE	NC TP CPU RSVD<43..32>
TRUE	TP CPU RSVD<27..26>	TRUE	NC TP CPU RSVD<27..26>
TRUE	TP CPU RSVD<24..15>	TRUE	NC TP CPU RSVD<24..15>
TRUE	TP CPU RSVD<2..1>	TRUE	NC TP CPU RSVD<2..1>
TRUE	TP CPU RSVD NCTF<8..5>	TRUE	NC TP CPU RSVD NCTF<8..5>

NC NO TESTS

NC TEST	NC CRT IG BLUE	TRUE	NC CRT IG BLUE
TRUE	NC CRT IG GREEN	TRUE	NC CRT IG GREEN
TRUE	NC CRT IG RED	TRUE	NC CRT IG RED
TRUE	NC CRT IG DDC CLK	TRUE	NC CRT IG DDC CLK
TRUE	NC CRT IG DDC DATA	TRUE	NC CRT IG DDC DATA
TRUE	NC CRT IG HSYNC	TRUE	NC CRT IG HSYNC
TRUE	NC CRT IG VSYNC	TRUE	NC CRT IG VSYNC
TRUE	NC LVDS IG CTRL CLK	TRUE	NC LVDS IG CTRL CLK
TRUE	NC LVDS IG CTRL DATA	TRUE	NC LVDS IG CTRL DATA
TRUE	NC PCH LVDS VBG	TRUE	NC PCH LVDS VBG

NC NO TESTS

TRUE	TP AUD GPIO 2	56
TRUE	TP AUD GPIO 1	56
TRUE	TP AUD L01 L N	56
TRUE	TP AUD L01 L P	56
TRUE	TP BKL FAULT	88
TRUE	TP SPI_DESCRIPTOR_OVERRIDE L	44
TRUE	TP XDPPCH HOOK2	23
TRUE	TP XDPPCH HOOK3	23
TRUE	TP GMUX PL6B	87
TRUE	PM RSMRST L	17
TRUE	CPUIVMV BOOT1	67
TRUE	CPUIVMV BOOT2	67
TRUE	CPUIVMV UGATE7	67
TRUE	TP LV05 S0 PCH VCCAPLEX	20

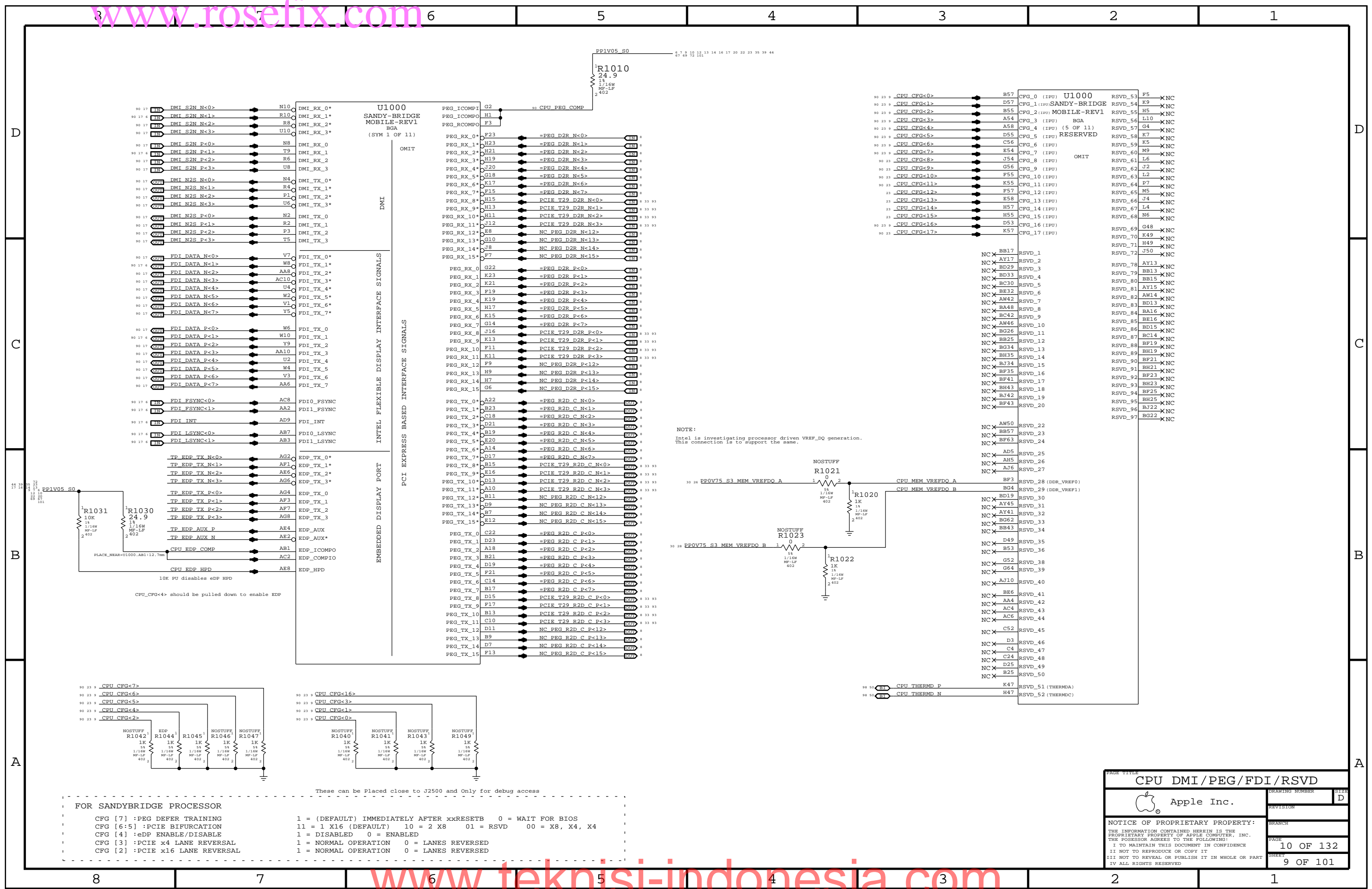
TRUE	NC PCI PME L	TRUE	NC PCI PME L
TRUE	NC PCI CLK33M OUT3	TRUE	NC PCI CLK33M OUT3
TRUE	NC PCIE CLK100M PE4N	TRUE	NC PCIE CLK100M PE4N
TRUE	NC PCIE CLK100M PE4P	TRUE	NC PCIE CLK100M PE4P
TRUE	NC PCIE CLK100M PE5N	TRUE	NC PCIE CLK100M PE5N
TRUE	NC PCIE CLK100M PE5P	TRUE	NC PCIE CLK100M PE5P
TRUE	NC PCIE CLK100M PE6N	TRUE	NC PCIE CLK100M PE6N
TRUE	NC PCIE CLK100M PE6P	TRUE	NC PCIE CLK100M PE6P
TRUE	NC PCIE CLK100M PE7N	TRUE	NC PCIE CLK100M PE7N
TRUE	NC PCIE CLK100M PE7P	TRUE	NC PCIE CLK100M PE7P
TRUE	NC PSOC P1 3	TRUE	NC PSOC P1 3
TRUE	NC SATA B D2RN	TRUE	NC SATA B D2RN
TRUE	NC SATA B D2RP	TRUE	NC SATA B D2RP
TRUE	NC SATA B R2D CN	TRUE	NC SATA B R2D CN
TRUE	NC SATA B R2D CP	TRUE	NC SATA B R2D CP
TRUE	NC SATA D D2RN	TRUE	NC SATA D D2RN
TRUE	NC SATA D D2RP	TRUE	NC SATA D D2RP
TRUE	NC SATA D R2D CN	TRUE	NC SATA D R2D CN
TRUE	NC SATA D R2D CP	TRUE	NC SATA D R2D CP
TRUE	NC SATA E D2RN	TRUE	NC SATA E D2RN
TRUE	NC SATA E D2RP	TRUE	NC SATA E D2RP
TRUE	NC SATA E R2D CN	TRUE	NC SATA E R2D CN
TRUE	NC SATA E R2D CP	TRUE	NC SATA E R2D CP
TRUE	NC SATA F D2RN	TRUE	NC SATA F D2RN
TRUE	NC SATA F D2RP	TRUE	NC SATA F D2RP
TRUE	NC SATA F R2D CN	TRUE	NC SATA F R2D CN
TRUE	NC SATA F R2D CP	TRUE	NC SATA F R2D CP

TP SMC P41

TRUE	TP SMC P41	TRUE	NC SMC P41
TRUE	NC LPC DREQ0 L	TRUE	NC LPC DREQ0 L
TRUE	NC CLINK CLK	TRUE	NC CLINK CLK
TRUE	NC CLINK DATA	TRUE	NC CLINK DATA
TRUE	NC CLINK RESET L	TRUE	NC CLINK RESET L
TRUE	NC PCIE CLK100M PE6N	TRUE	NC PCIE CLK100M PE6N
TRUE	NC PCIE CLK100M PE6P	TRUE	NC PCIE CLK100





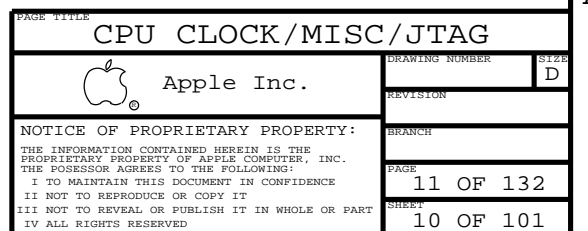


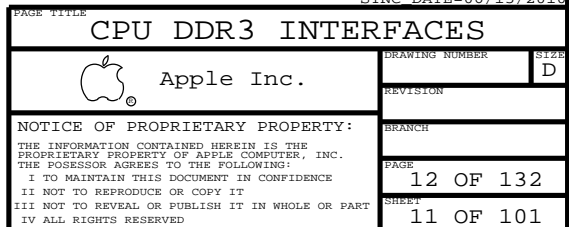
FOR SANDYBRIDGE PROCESSOR

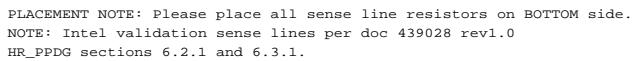
CFG [7] :PEG DEFER TRAINING
CFG [6:5] :PCIE BIFURCATION
CFG [4] :eDP ENABLE/DISABLE
CFG [3] :PCIE x4 LANE REVERSAL
CFG [2] :PCIE x16 LANE REVERSAL

1 = (DEFAULT) IMMEDIATELY AFTER xxRESETB 0 = WAIT FOR BIOS
11 = 1 X16 (DEFAULT) 10 = 2 X8 01 = RSVD 00 = X8, X4, X4
1 = DISABLED 0 = ENABLED
1 = NORMAL OPERATION 0 = LANES REVERSED
1 = NORMAL OPERATION 0 = LANES REVERSED

CPU DMI/PEG/FDI/RSVD	
Apple Inc.	DRAWING NUMBER
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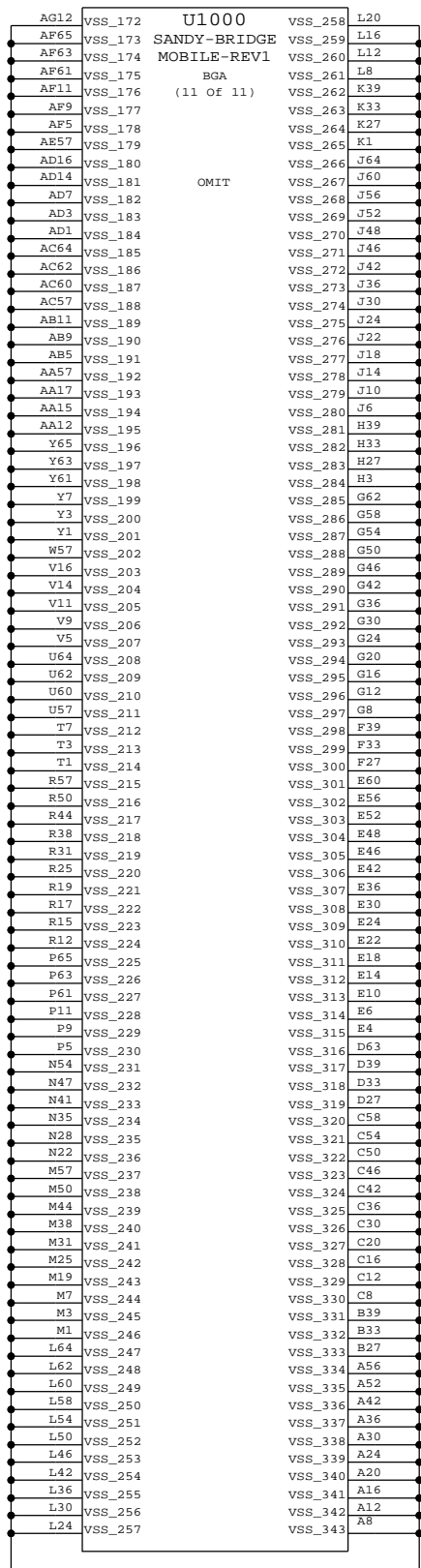
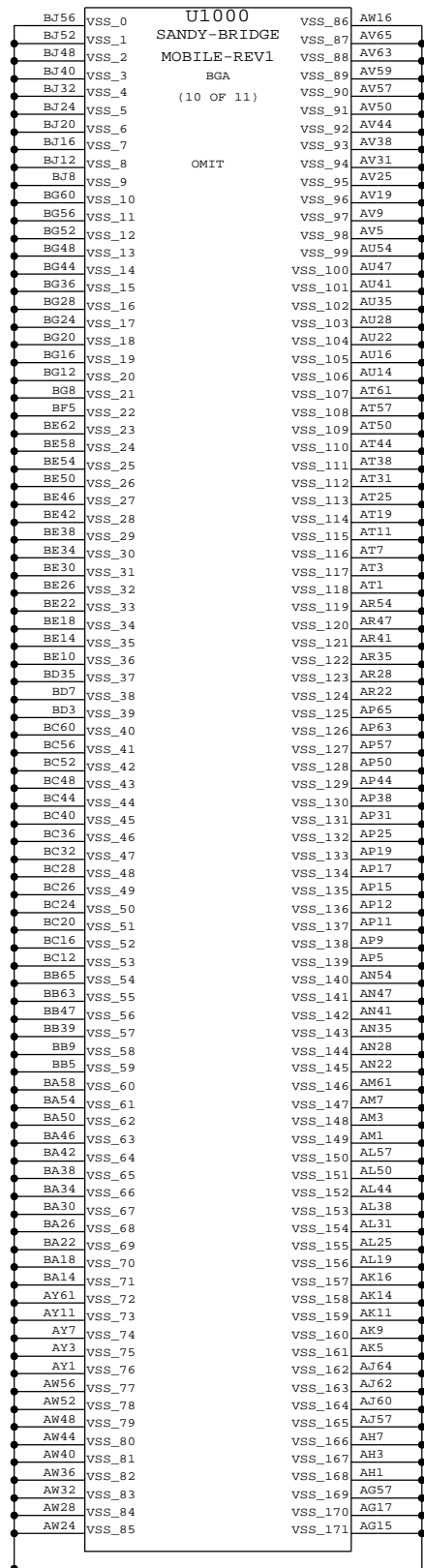


D

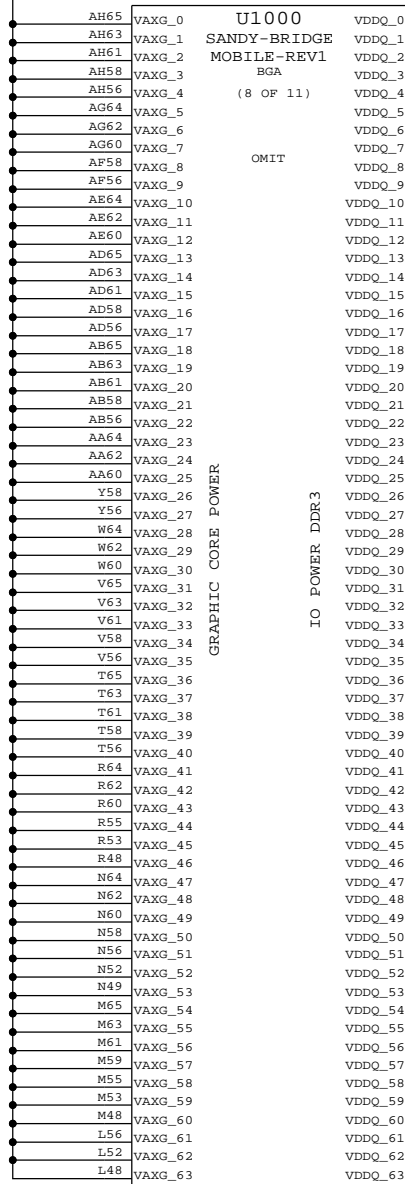
C

B

A

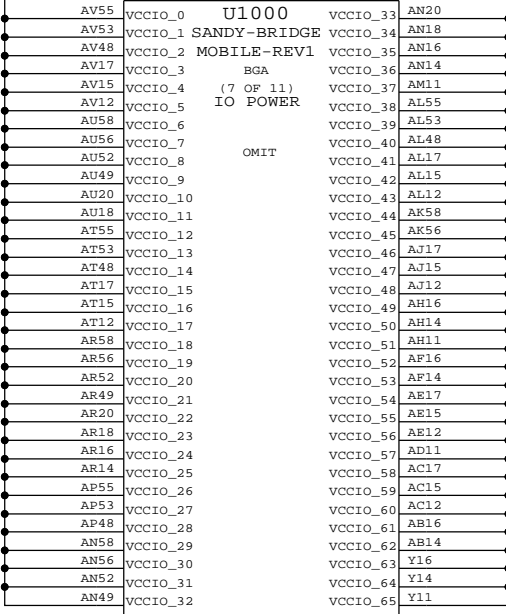


PPVCORE_S0_AXG



PP1V5_S3RS0_CPUDDR

PP1V05_S0



PP1V05_S0

CPU POWER AND GND		
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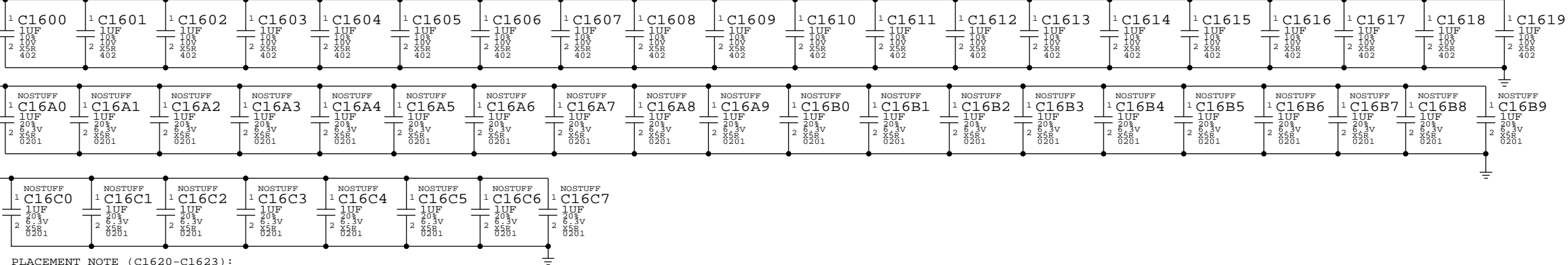
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CPU VCORE DECOUPLING

Intel recommendation: 4x 470uF 4mOhm, 2x 470uF 4mOhm (NOSTUFF), 16x 22uF 0805, 4x 10uF 0603, 20x 1uF 0402, 28x 1uF 0402 (NOSTUFF)
Apple Implementation: 4x 470uF 4mOhm, 1x 470uF 4mOhm (NOSTUFF), 16x 22uF 0603, 4x 10uF 0402, 20x 1uF 0402, 28x 1uF 0201 (NOSTUFF), 4x 22uF 0603 (NOSTUFF)

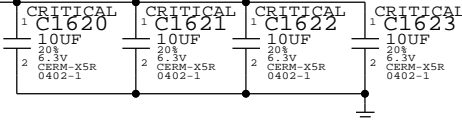
PLACEMENT_NOTE (C1600-C16C7):

Place on bottom side of U1000



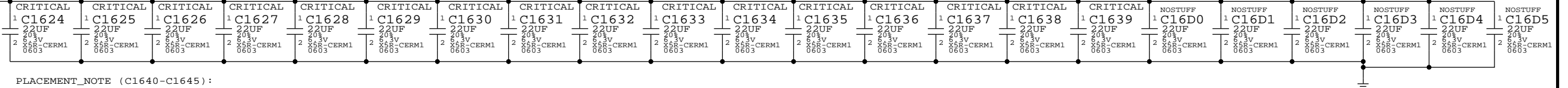
PLACEMENT_NOTE (C1620-C1623):

Place near U1000 on bottom side



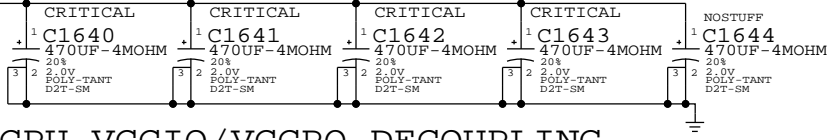
PLACEMENT_NOTE (C1624-C16D5):

Place near inductors on bottom side



PLACEMENT_NOTE (C1640-C1645):

Place near inductors on bottom side.

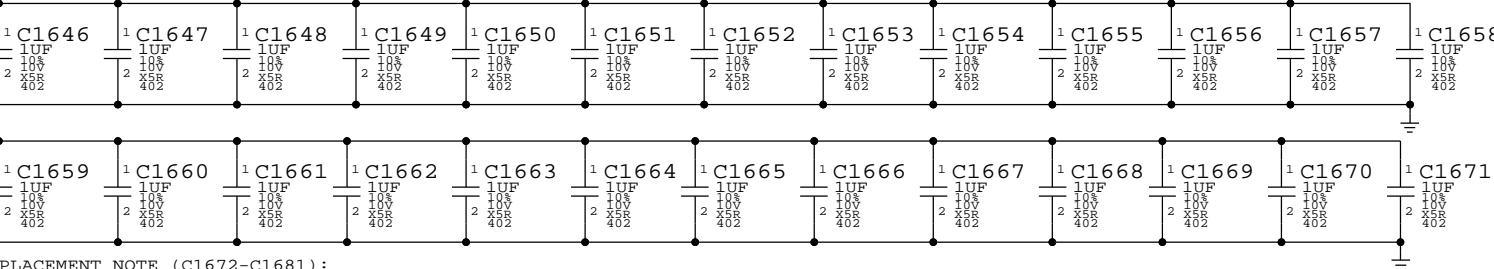


CPU VCCIO/VCCPQ DECOUPLING

Intel recommendation: 2x 330uF, 10x 10uF 0603, 26x 1uF 0402
Apple Implementation: 2x 330uF, 10x 10uF 0603, 26x 1uF 0402

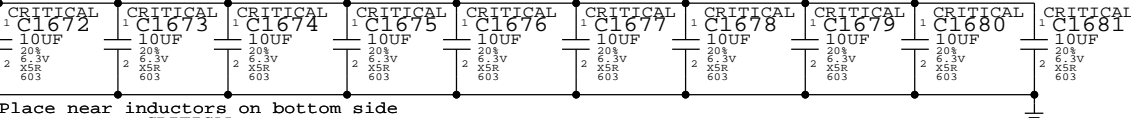
PLACEMENT_NOTE (C1646-C1671):

Place on bottom side of U1000

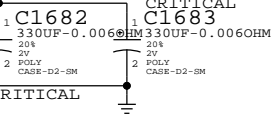


PLACEMENT_NOTE (C1672-C1681):

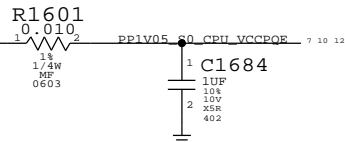
Place near U1000 on bottom side



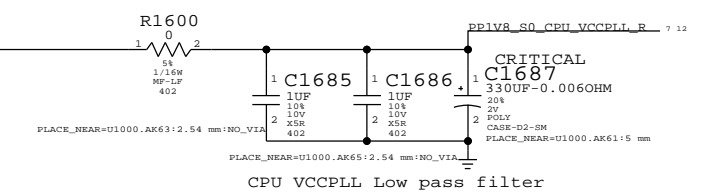
Place near inductors on bottom side



Intel recommendation: 1x 10mOhm resistor, 1x 1uF 0402



CPU VCCPLL DECOUPLING



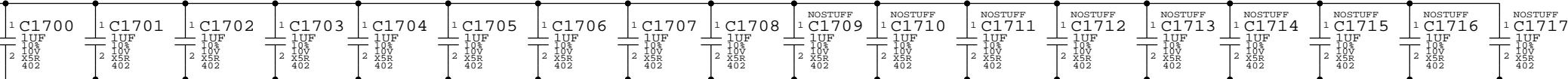
CPU VCCPLL Low pass filter

SYNC MASTER=K92 MLB		SYNC DATE=08/19/2010	
PAGE TITLE		CPU DECOUPLING-I	
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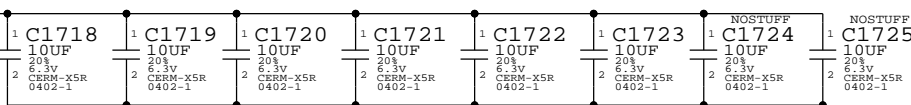
VAXG DECOUPLING

Intel recommendation: 2x 470uF 4mOhm, 2x 470uF 4mOhm (NOSTUFF), 6x 22uF 0805, 2x 22uF 0805 (NOSTUFF), 6x 10uF 0603, 2x 10uF 0603 (NOSTUFF), 9x 1uF 0402, 9x 1uF 0402 (NOSTUFF)
Apple Implementation: 2x 470uF 4mOhm, 1x 470uF 4mOhm (NOSTUFF), 6x 22uF 0603, 2x 22uF 0603 (NOSTUFF), 6x 10uF 0402, 2x 10uF 0402 (NOSTUFF), 9x 1uF 0402, 9x 1uF 0402 (NOSTUFF)

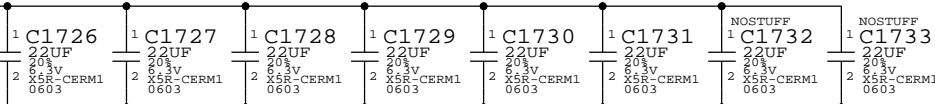
PLACEMENT_NOTE (C1700-C1708):
Place on bottom side of U1000



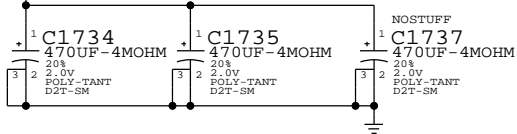
PLACEMENT_NOTE (C1718-C1723):
Place close to U1000 on bottom side



PLACEMENT_NOTE (C1726-C1731):
Place near inductors on bottom side.



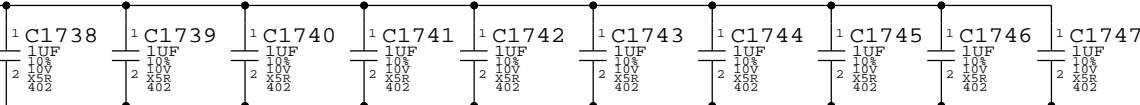
PLACEMENT_NOTE (C1734-C1735):
Place near inductors on bottom side.



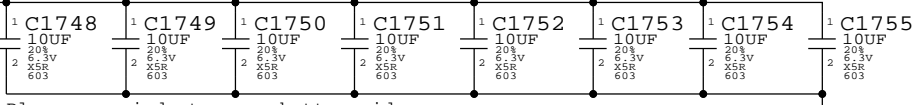
CPU VDDQ/VCCDQ DECOUPLING

Intel recommendation: 1x 330uF, 8x 10uF 0603, 10x 1uF 0402
Apple Implementation: 1x 330uF, 8x 10uF 0603, 10x 1uF 0402

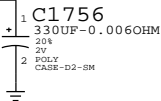
PLACEMENT_NOTE (C1738-C1747):
Place on bottom side of U1000



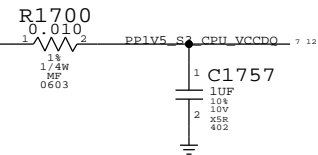
Place close to U1000 on bottom side



Place near inductors on bottom side



Intel recommendation: 1x 10mOhm resistor, 1x 1uF 0402

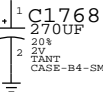
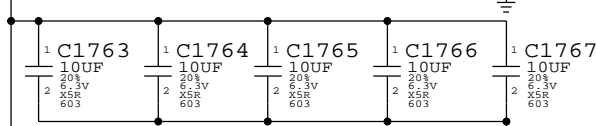
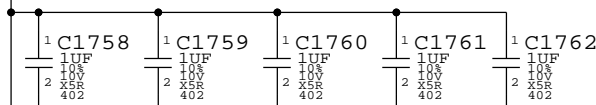


CPU VCCSA DECOUPLING


Intel recommendation: 1x 330uF, 5x 10uF 0603, 5x 1uF 0402
Apple Implementation: 1x 330uF, 5x 10uF 0603, 5x 1uF 0402

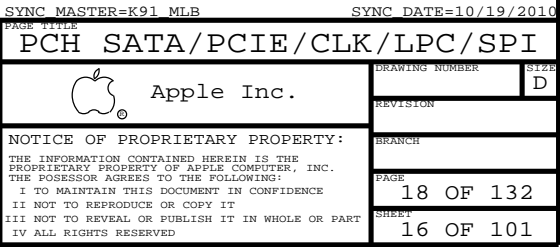
PLACEMENT_NOTE (C1758-C1762):

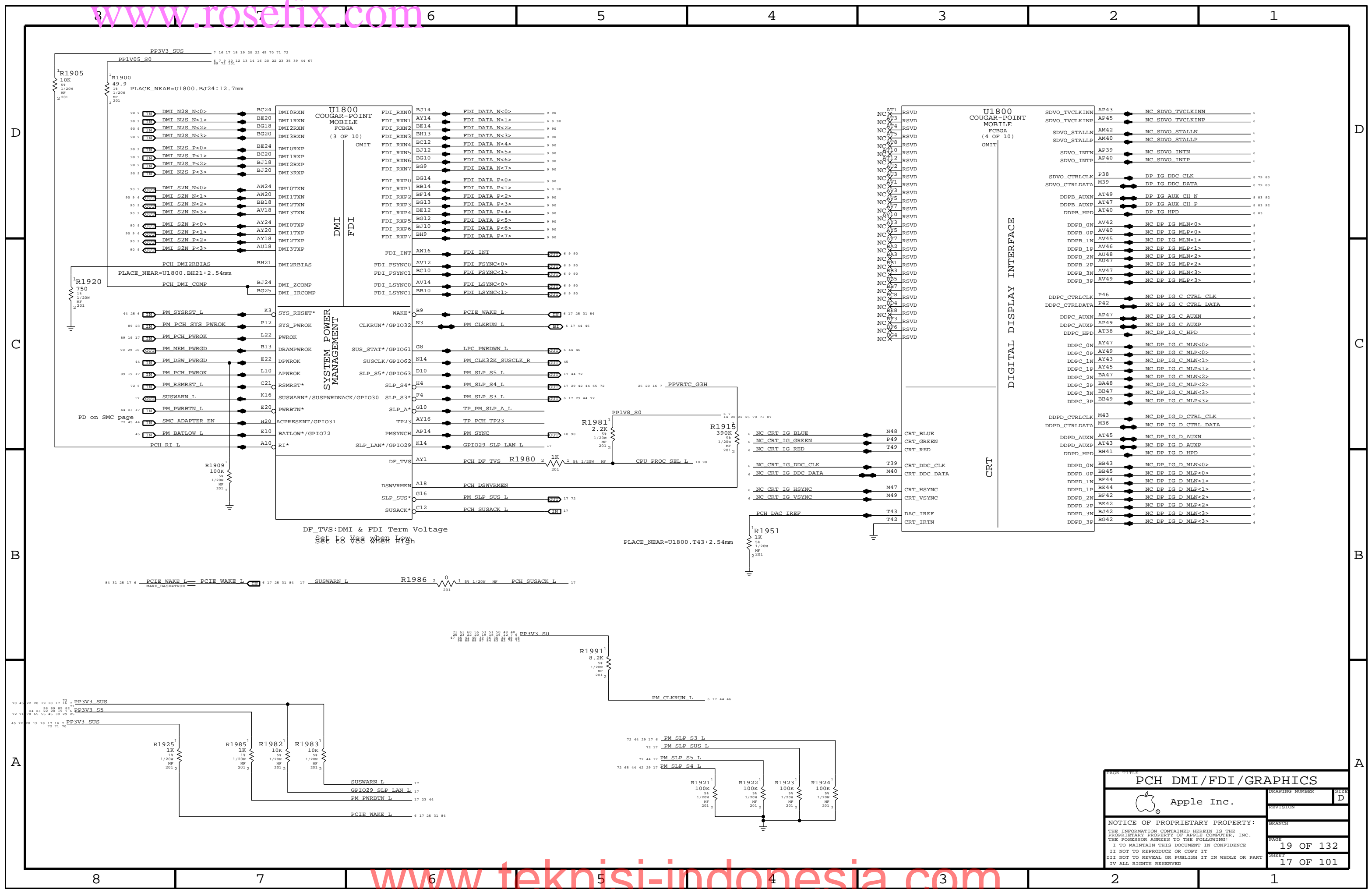
Place on bottom side of U1000

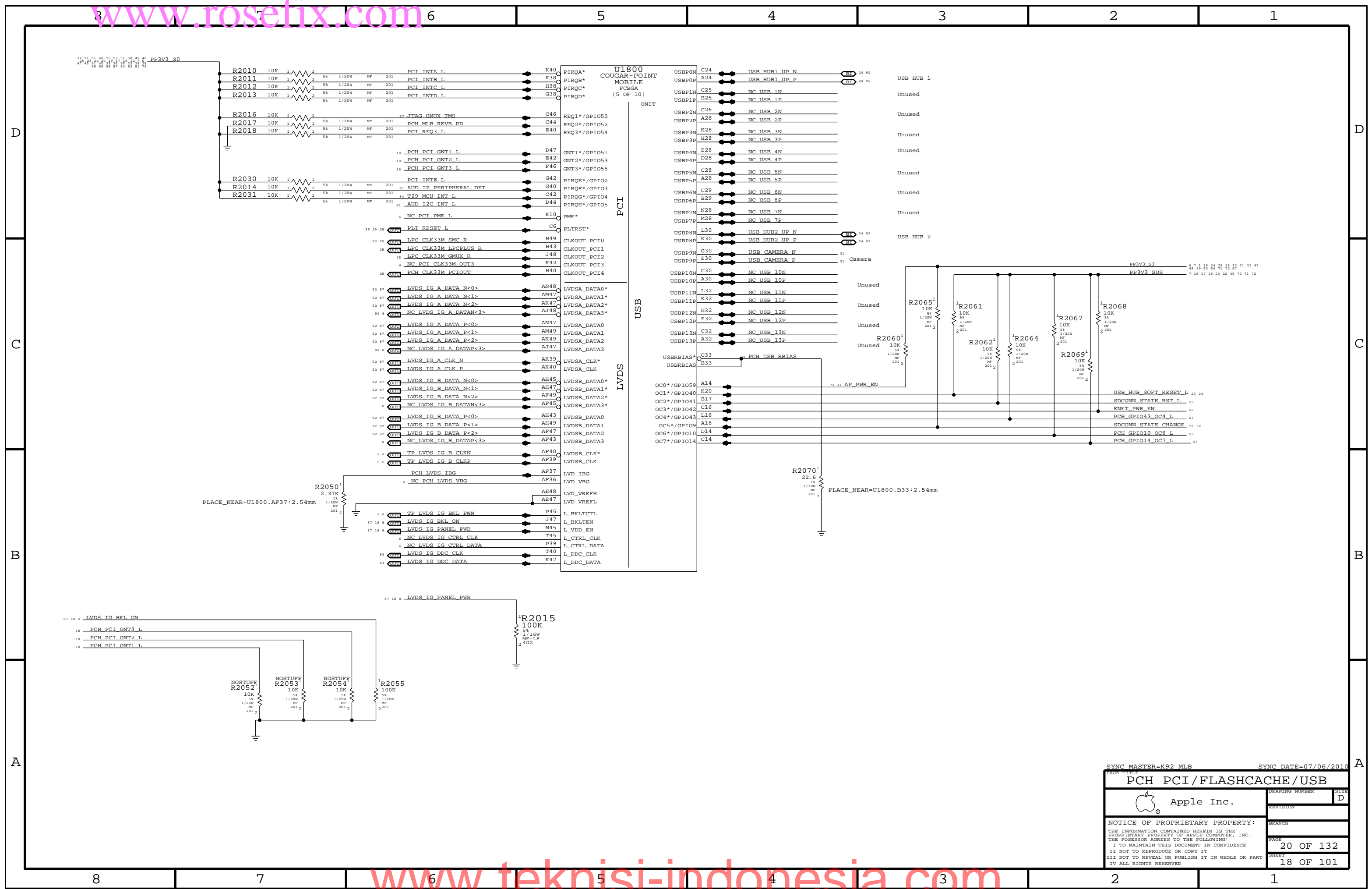


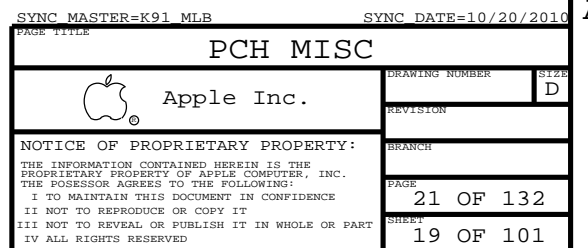
SYNC MASTER=K92 MLB SYNC DATE=08/19/2010

PAGE TITLE		
CPU DECOUPLING-II		
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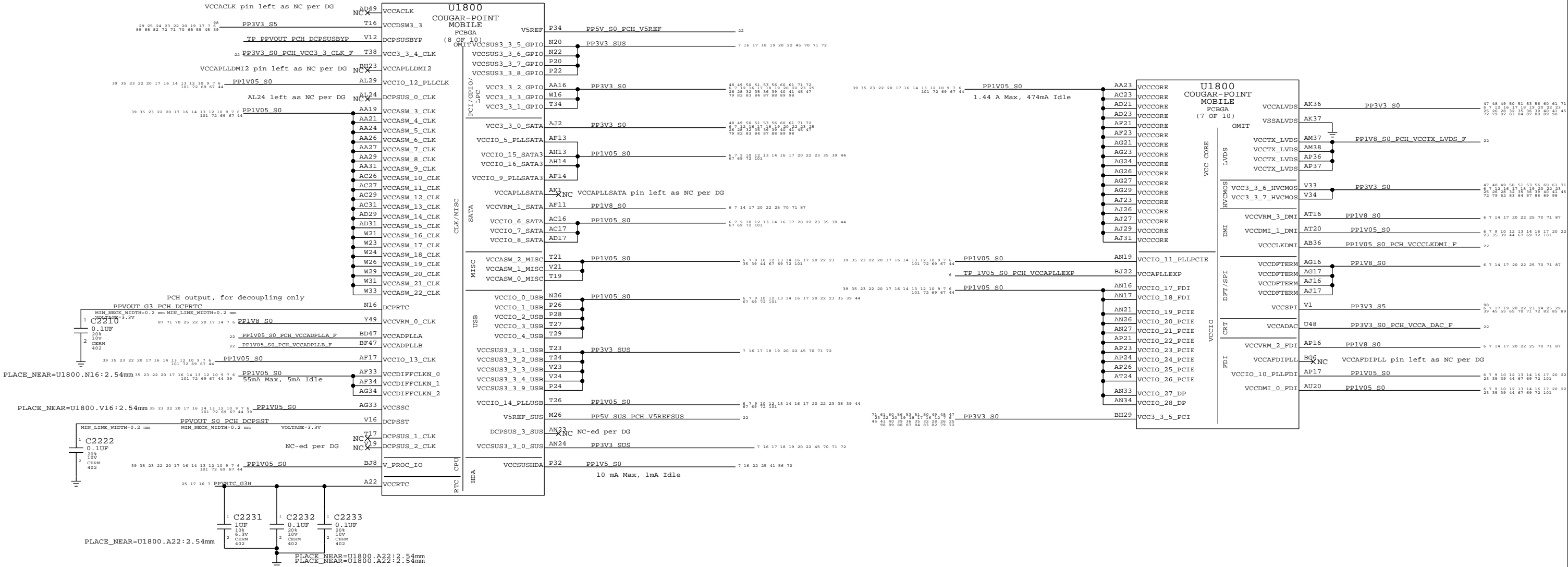


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D

C

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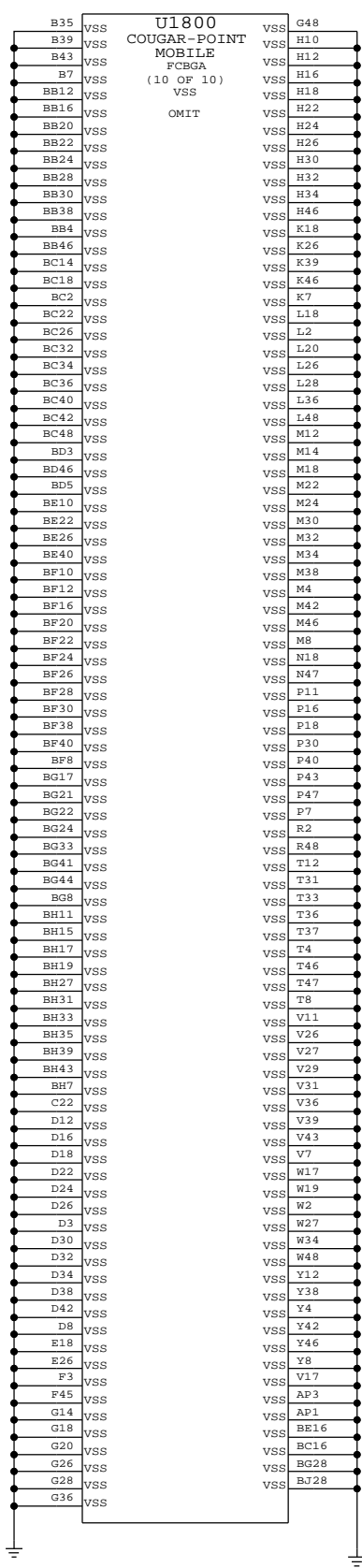
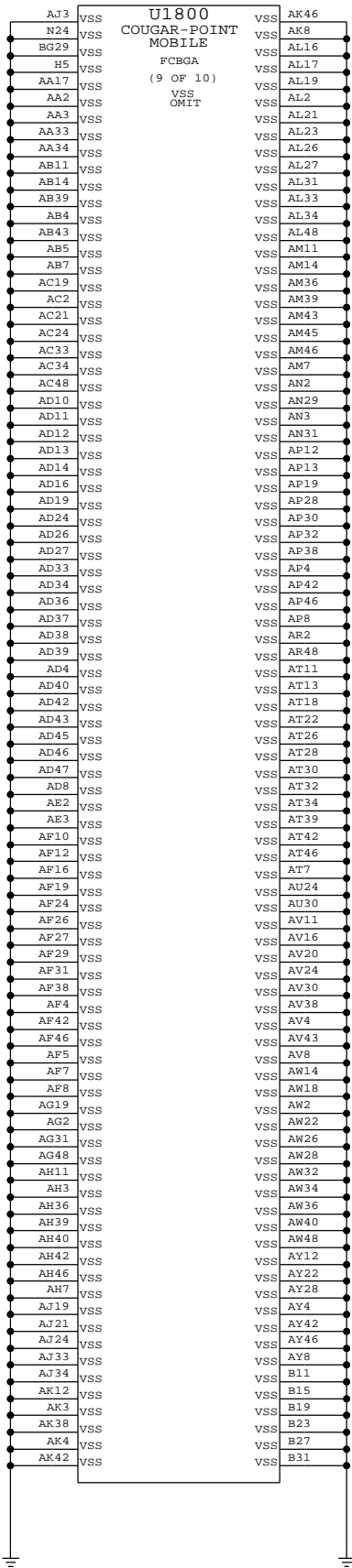
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D

C

B

A



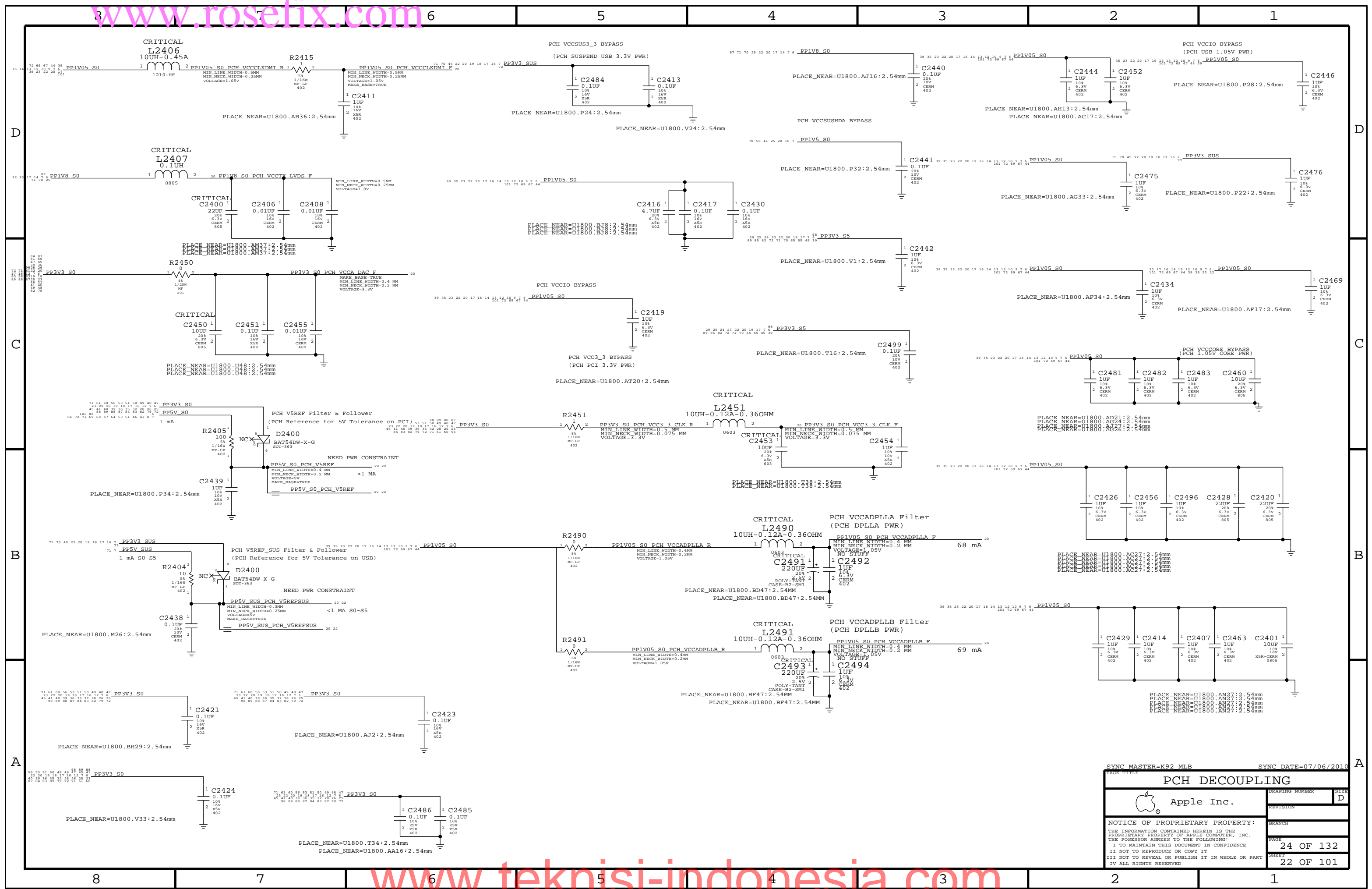
D

C

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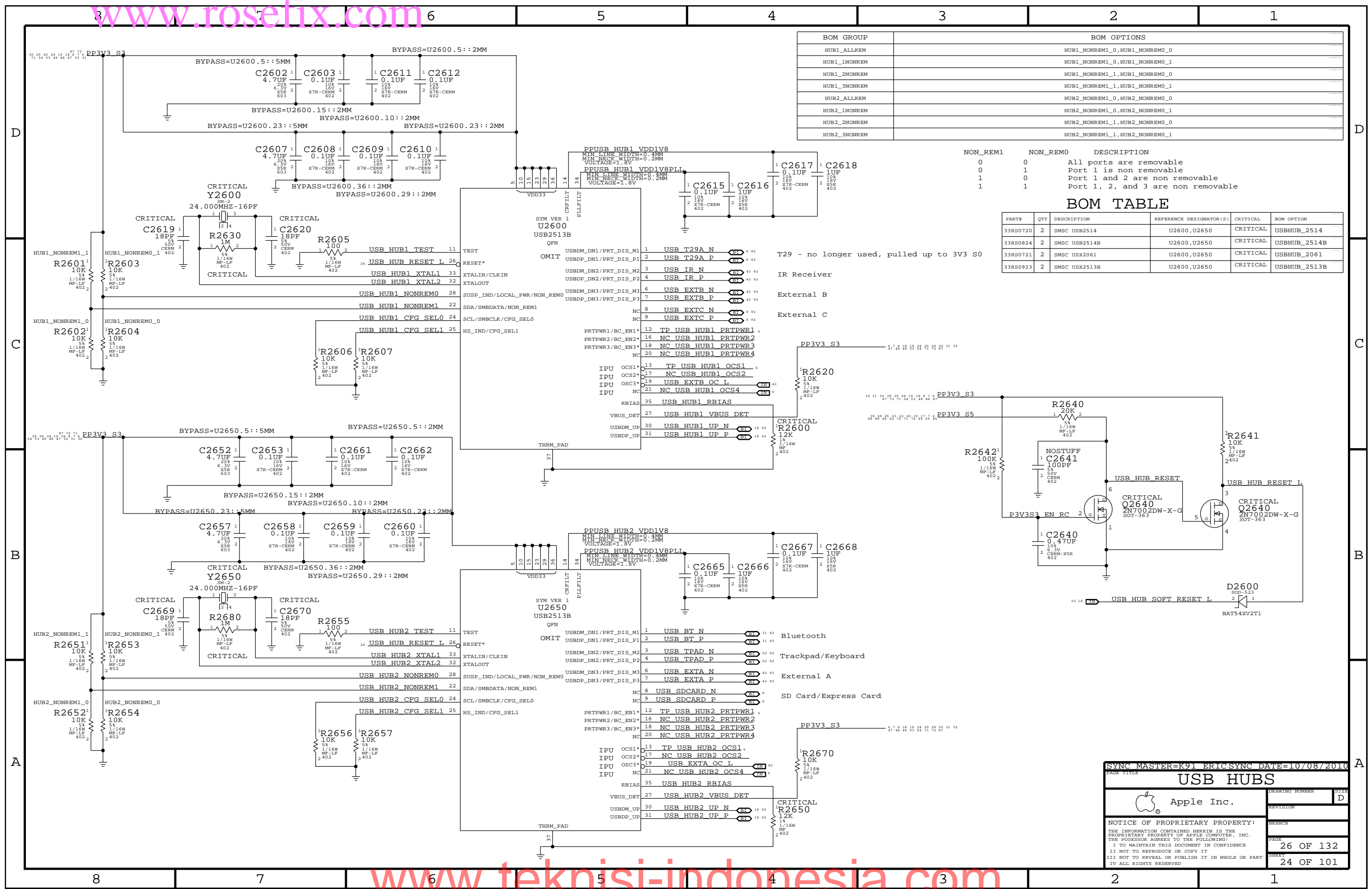
A

PAGE TITLE		SYNC MASTER=K92 MLB		SYNC DATE=04/30/2010	
PCH GROUNDS				DRAWING NUMBER	SIZE
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SYNC MASTER=K92 MLB		SYNC DATE=07/06/2010	
PAGE TITLE		PCH DECOUPLING	
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BOM GROUP	BOM OPTIONS
HUB1_ALLREM	HUB1_NONREM1_0, HUB1_NONREM0_0
HUB1_1NONREM	HUB1_NONREM1_0, HUB1_NONREM0_1
HUB1_2NONREM	HUB1_NONREM1_1, HUB1_NONREM0_0
HUB1_3NONREM	HUB1_NONREM1_1, HUB1_NONREM0_1
HUB2_ALLREM	HUB2_NONREM1_0, HUB2_NONREM0_0
HUB2_1NONREM	HUB2_NONREM1_0, HUB2_NONREM0_1
HUB2_2NONREM	HUB2_NONREM1_1, HUB2_NONREM0_0
HUB2_3NONREM	HUB2_NONREM1_1, HUB2_NONREM0_1

NON_REM1	NON_REM0	DESCRIPTION
0	0	All ports are removable
0	1	Port 1 is non removable
1	0	Port 1 and 2 are non removable
1	1	Port 1, 2, and 3 are non removable

BOM TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0720	2	SMSC USB2514	U2600, U2650	CRITICAL	USBHUB_2514
338S0824	2	SMSC USB2514B	U2600, U2650	CRITICAL	USBHUB_2514B
338S0721	2	SMSC USX2061	U2600, U2650	CRITICAL	USBHUB_2061
338S0923	2	SMSC USX2513B	U2600, U2650	CRITICAL	USBHUB_2513B

T29 - no longer used, pulled up to 3V3 S0

IR Receiver

External B

External C


Bluetooth

Trackpad/Keyboard

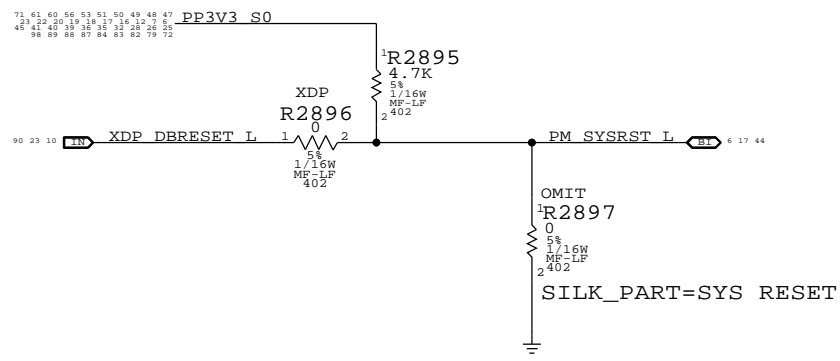
External A

SD Card/Express Card

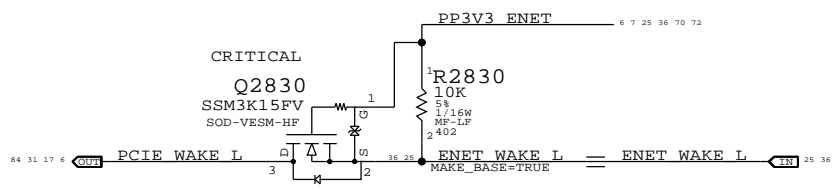
SYNC MASTER=K91 ERICS SYNC DATE=10/08/2010

PAGE TITLE		
USB HUBS		
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	PAGE	26 OF 132
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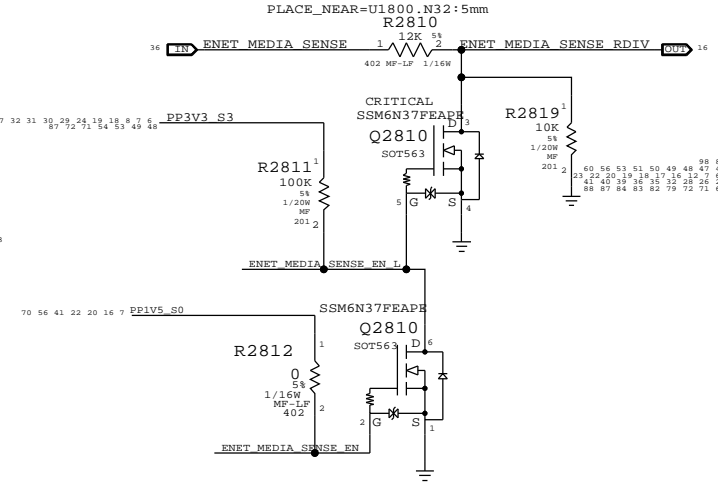
PCH Reset Button



Ethernet WAKE# Isolation

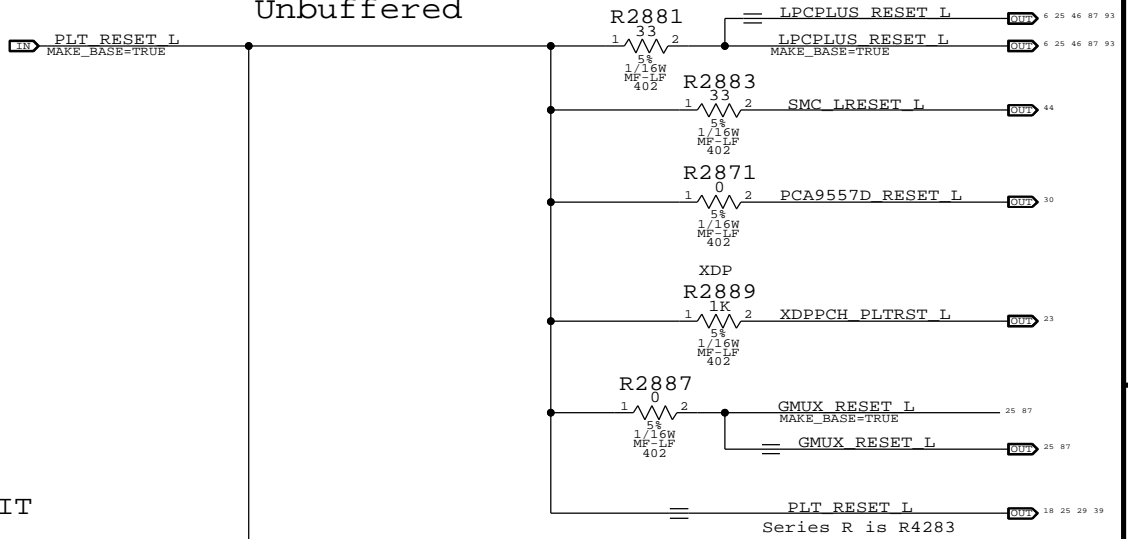


ENET_MEDIA_SENSE ISOLATION CIRCUIT



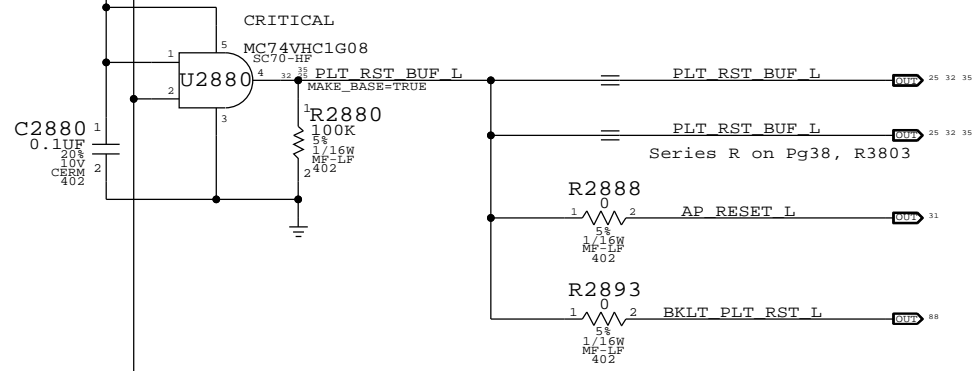
Platform Reset Connections

Unbuffered



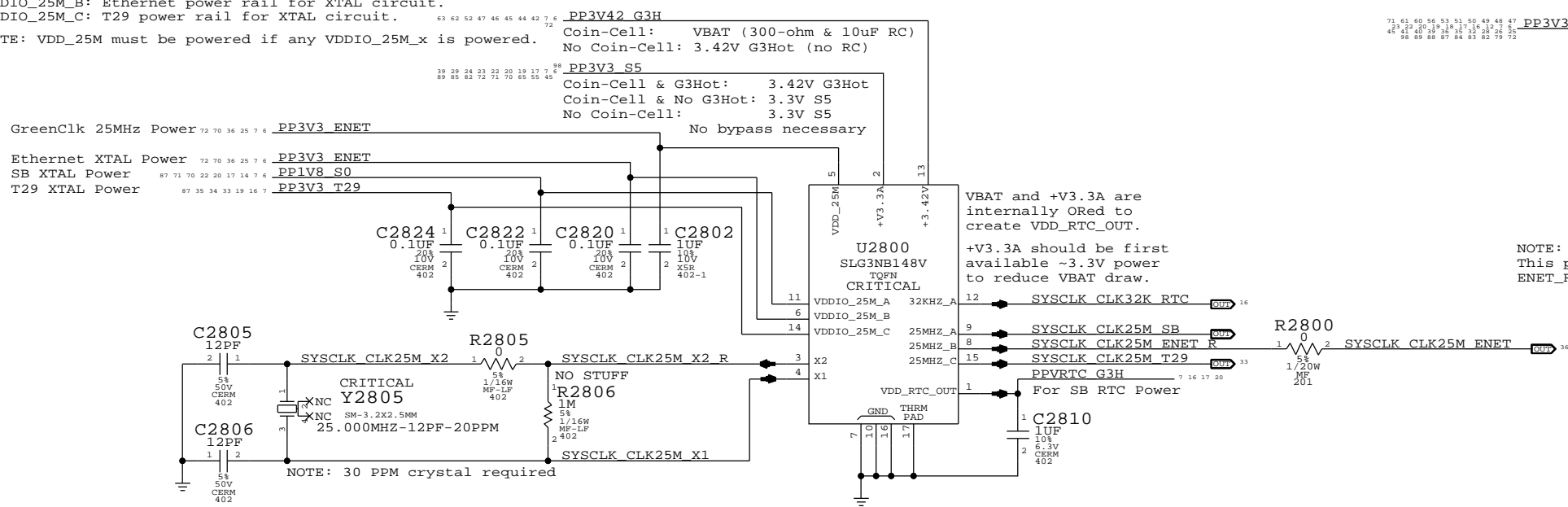
Buffered

Note: Based on K91/K92 layout, ENET,AP and BKLT are moved to Buffered reset.

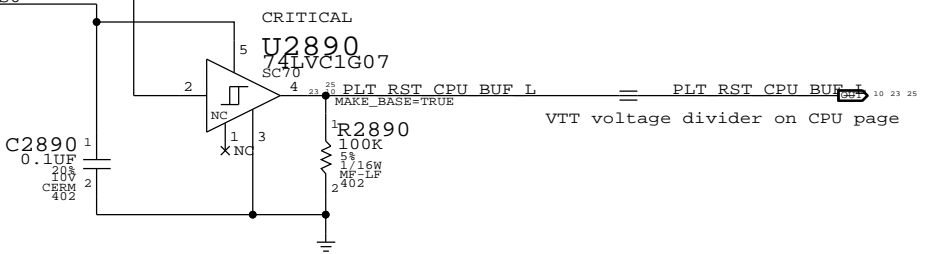


System RTC Power Source & 32kHz / 25MHz Clock Generator


VDDIO_25M_A: SB power rail for XTAL circuit.
VDDIO_25M_B: Ethernet power rail for XTAL circuit.
VDDIO_25M_C: T29 power rail for XTAL circuit.
NOTE: VDD_25M must be powered if any VDDIO_25M_x is powered.



Buffered CPU reset



NOTE:
This page is different for K92.
ENET_RESET_L hooked up differently on both the projects.

SYNC MASTER=K92 MLB		SYNC DATE=07/06/2010	
PAGE TITLE			
Chipset Support			
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Page Notes

Power aliases required by this page:

- =PP1V5_S0_MEM_A
- =PP1V5_S3_MEM_A
- =PP0V75_S0_MEM_VTT_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:

- =I2C_S0DIMM_SCL
- =I2C_S0DIMM_SDA

BOM options provided by this page:

(NONE)

DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

71 66 29 28 7 6 PP1V5_S3

PLACE_NEAR=J2900.75:2.54mm

PLACE_NEAR=J2900.75:2.54mm

PLACE_NEAR=J2900.75:2.54mm

PLACE_NEAR=J2900.75:2.54mm

PLACE_NEAR=J2900.75:2.54mm

PLACE_NEAR=J2900.75:2.54mm

PLACE_NEAR=J2900.75:2.54mm

PLACE_NEAR=J2900.75:2.54mm

PLACE_NEAR=J2900.75:2.54mm

30 9 PP0V75_S3 MEM VREFDQ_A

PLACE_NEAR=J2900.75:2.54mm

OMIT_TABLE

CRITICAL

J2900

F-RT-THB

DDR3-SODIMM-DUAL-K6

(SYMBOL 1 OF 2)

See CSA05 BOM table

PP0V75_S3 MEM VREFCA_A

PP0V75_S0 DDRVTT

"Factory" (top) slot

516-0229

SPD_ADDR=0xA0 (WR) / 0xA1 (RD)

SYNC MASTER=K92 SUMA		SYNC DATE=06/23/2010	
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DDR3 SO-DIMM Connector A			
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C

B

A

CPU CHANNEL A DQS 0 -> DIMM A DQS 0			
91 11 6	MEM A DQS N<0>	==	=MEM A DQS N<0>
91 11 6	MEM A DQS P<0>	==	=MEM A DQS P<0>
91 11 6	MEM A DQ<7>	==	=MEM A DQ<3>
91 11 6	MEM A DQ<6>	==	=MEM A DQ<6>
91 11 6	MEM A DQ<5>	==	=MEM A DQ<5>
91 11 6	MEM A DQ<4>	==	=MEM A DQ<4>
91 11 6	MEM A DQ<3>	==	=MEM A DQ<7>
91 11 6	MEM A DQ<2>	==	=MEM A DQ<0>
91 11 6	MEM A DQ<1>	==	=MEM A DQ<1>
91 11 6	MEM A DQ<0>	==	=MEM A DQ<2>
CPU CHANNEL A DQS 1 -> DIMM A DQS 1			
91 11 6	MEM A DQS N<1>	==	=MEM A DQS N<1>
91 11 6	MEM A DQS P<1>	==	=MEM A DQS P<1>
91 11 6	MEM A DQ<15>	==	=MEM A DQ<15>
91 11 6	MEM A DQ<14>	==	=MEM A DQ<14>
91 11 6	MEM A DQ<13>	==	=MEM A DQ<12>
91 11 6	MEM A DQ<12>	==	=MEM A DQ<13>
91 11 6	MEM A DQ<11>	==	=MEM A DQ<10>
91 11 6	MEM A DQ<10>	==	=MEM A DQ<11>
91 11 6	MEM A DQ<9>	==	=MEM A DQ<9>
91 11 6	MEM A DQ<8>	==	=MEM A DQ<8>
CPU CHANNEL A DQS 2 -> DIMM A DQS 2			
91 11 6	MEM A DQS N<2>	==	=MEM A DQS N<2>
91 11 6	MEM A DQS P<2>	==	=MEM A DQS P<2>
91 11 6	MEM A DQ<23>	==	=MEM A DQ<23>
91 11 6	MEM A DQ<22>	==	=MEM A DQ<22>
91 11 6	MEM A DQ<21>	==	=MEM A DQ<17>
91 11 6	MEM A DQ<20>	==	=MEM A DQ<20>
91 11 6	MEM A DQ<19>	==	=MEM A DQ<19>
91 11 6	MEM A DQ<18>	==	=MEM A DQ<18>
91 11 6	MEM A DQ<17>	==	=MEM A DQ<16>
91 11 6	MEM A DQ<16>	==	=MEM A DQ<21>
CPU CHANNEL A DQS 3 -> DIMM A DQS 3			
91 11 6	MEM A DQS N<3>	==	=MEM A DQS N<3>
91 11 6	MEM A DQS P<3>	==	=MEM A DQS P<3>
91 11 6	MEM A DQ<31>	==	=MEM A DQ<31>
91 11 6	MEM A DQ<30>	==	=MEM A DQ<30>
91 11 6	MEM A DQ<29>	==	=MEM A DQ<29>
91 11 6	MEM A DQ<28>	==	=MEM A DQ<28>
91 11 6	MEM A DQ<27>	==	=MEM A DQ<27>
91 11 6	MEM A DQ<26>	==	=MEM A DQ<26>
91 11 6	MEM A DQ<25>	==	=MEM A DQ<25>
91 11 6	MEM A DQ<24>	==	=MEM A DQ<24>
CPU CHANNEL A DQS 4 -> DIMM A DQS 4			
91 11 6	MEM A DQS N<4>	==	=MEM A DQS N<4>
91 11 6	MEM A DQS P<4>	==	=MEM A DQS P<4>
91 11 6	MEM A DQ<39>	==	=MEM A DQ<38>
91 11 6	MEM A DQ<38>	==	=MEM A DQ<37>
91 11 6	MEM A DQ<37>	==	=MEM A DQ<39>
91 11 6	MEM A DQ<36>	==	=MEM A DQ<33>
91 11 6	MEM A DQ<35>	==	=MEM A DQ<35>
91 11 6	MEM A DQ<34>	==	=MEM A DQ<34>
91 11 6	MEM A DQ<33>	==	=MEM A DQ<32>
91 27 26 11 6	MEM A DQ<32>	==	MEM A DQ<32>
CPU CHANNEL A DQS 5 -> DIMM A DQS 5			
91 11 6	MEM A DQS N<5>	==	=MEM A DQS N<5>
91 11 6	MEM A DQS P<5>	==	=MEM A DQS P<5>
91 11 6	MEM A DQ<47>	==	=MEM A DQ<47>
91 11 6	MEM A DQ<46>	==	=MEM A DQ<41>
91 11 6	MEM A DQ<45>	==	=MEM A DQ<43>
91 11 6	MEM A DQ<44>	==	=MEM A DQ<44>
91 11 6	MEM A DQ<43>	==	=MEM A DQ<40>
91 11 6	MEM A DQ<42>	==	=MEM A DQ<46>
91 11 6	MEM A DQ<41>	==	=MEM A DQ<42>
91 11 6	MEM A DQ<40>	==	=MEM A DQ<45>
CPU CHANNEL A DQS 6 -> DIMM A DQS 6			
91 27 26 11 6	MEM A DQS N<6>	==	MEM A DQS N<6>
91 27 26 11 6	MEM A DQS P<6>	==	MEM A DQS P<6>
91 11 6	MEM A DQ<55>	==	=MEM A DQ<49>
91 11 6	MEM A DQ<54>	==	=MEM A DQ<54>
91 11 6	MEM A DQ<53>	==	=MEM A DQ<55>
91 11 6	MEM A DQ<52>	==	=MEM A DQ<52>
91 11 6	MEM A DQ<51>	==	=MEM A DQ<51>
91 11 6	MEM A DQ<50>	==	=MEM A DQ<50>
91 11 6	MEM A DQ<49>	==	=MEM A DQ<53>
91 11 6	MEM A DQ<48>	==	=MEM A DQ<48>
CPU CHANNEL A DQS 7 -> DIMM A DQS 7			
91 11 6	MEM A DQS N<7>	==	=MEM A DQS N<7>
91 11 6	MEM A DQS P<7>	==	=MEM A DQS P<7>
91 11 6	MEM A DQ<63>	==	=MEM A DQ<59>
91 11 6	MEM A DQ<62>	==	=MEM A DQ<58>
91 11 6	MEM A DQ<61>	==	=MEM A DQ<56>
91 11 6	MEM A DQ<60>	==	=MEM A DQ<61>
91 11 6	MEM A DQ<59>	==	=MEM A DQ<63>
91 11 6	MEM A DQ<58>	==	=MEM A DQ<62>
91 11 6	MEM A DQ<57>	==	=MEM A DQ<57>
91 11 6	MEM A DQ<56>	==	=MEM A DQ<60>


CPU CHANNEL B DQS 0 -> DIMM B DQS 0			
91 11 6	MEM B DQS N<0>	==	=MEM B DQS N<0>
91 11 6	MEM B DQS P<0>	==	=MEM B DQS P<0>
91 11 6	MEM B DQ<7>	==	=MEM B DQ<6>
91 11 6	MEM B DQ<6>	==	=MEM B DQ<3>
91 11 6	MEM B DQ<5>	==	=MEM B DQ<5>
91 11 6	MEM B DQ<4>	==	=MEM B DQ<4>
91 11 6	MEM B DQ<3>	==	=MEM B DQ<1>
91 11 6	MEM B DQ<2>	==	=MEM B DQ<7>
91 11 6	MEM B DQ<1>	==	=MEM B DQ<2>
91 11 6	MEM B DQ<0>	==	=MEM B DQ<0>
CPU CHANNEL B DQS 1 -> DIMM B DQS 1			
91 11 6	MEM B DQS N<1>	==	=MEM B DQS N<1>
91 11 6	MEM B DQS P<1>	==	=MEM B DQS P<1>
91 11 6	MEM B DQ<15>	==	=MEM B DQ<15>
91 11 6	MEM B DQ<14>	==	=MEM B DQ<14>
91 11 6	MEM B DQ<13>	==	=MEM B DQ<13>
91 11 6	MEM B DQ<12>	==	=MEM B DQ<12>
91 11 6	MEM B DQ<11>	==	=MEM B DQ<11>
91 11 6	MEM B DQ<10>	==	=MEM B DQ<10>
91 11 6	MEM B DQ<9>	==	=MEM B DQ<9>
91 11 6	MEM B DQ<8>	==	=MEM B DQ<8>
CPU CHANNEL B DQS 2 -> DIMM B DQS 2			
91 11 6	MEM B DQS N<2>	==	=MEM B DQS N<2>
91 11 6	MEM B DQS P<2>	==	=MEM B DQS P<2>
91 11 6	MEM B DQ<23>	==	=MEM B DQ<23>
91 11 6	MEM B DQ<22>	==	=MEM B DQ<22>
91 11 6	MEM B DQ<21>	==	=MEM B DQ<21>
91 11 6	MEM B DQ<20>	==	=MEM B DQ<20>
91 11 6	MEM B DQ<19>	==	=MEM B DQ<19>
91 11 6	MEM B DQ<18>	==	=MEM B DQ<18>
91 11 6	MEM B DQ<17>	==	=MEM B DQ<17>
91 11 6	MEM B DQ<16>	==	=MEM B DQ<16>
CPU CHANNEL B DQS 3 -> DIMM B DQS 3			
91 11 6	MEM B DQS N<3>	==	=MEM B DQS N<3>
91 11 6	MEM B DQS P<3>	==	=MEM B DQS P<3>
91 11 6	MEM B DQ<31>	==	=MEM B DQ<31>
91 11 6	MEM B DQ<30>	==	=MEM B DQ<30>
91 11 6	MEM B DQ<29>	==	=MEM B DQ<29>
91 11 6	MEM B DQ<28>	==	=MEM B DQ<28>
91 11 6	MEM B DQ<27>	==	=MEM B DQ<27>
91 11 6	MEM B DQ<26>	==	=MEM B DQ<26>
91 11 6	MEM B DQ<25>	==	=MEM B DQ<25>
91 11 6	MEM B DQ<24>	==	=MEM B DQ<24>
CPU CHANNEL B DQS 4 -> DIMM B DQS 4			
91 11 6	MEM B DQS N<4>	==	=MEM B DQS N<4>
91 11 6	MEM B DQS P<4>	==	=MEM B DQS P<4>
91 11 6	MEM B DQ<39>	==	=MEM B DQ<39>
91 11 6	MEM B DQ<38>	==	=MEM B DQ<38>
91 11 6	MEM B DQ<37>	==	=MEM B DQ<37>
91 11 6	MEM B DQ<36>	==	=MEM B DQ<36>
91 11 6	MEM B DQ<35>	==	=MEM B DQ<35>
91 11 6	MEM B DQ<34>	==	=MEM B DQ<34>
91 11 6	MEM B DQ<33>	==	=MEM B DQ<33>
91 11 6	MEM B DQ<32>	==	=MEM B DQ<32>
CPU CHANNEL B DQS 5 -> DIMM B DQS 5			
91 11 6	MEM B DQS N<5>	==	=MEM B DQS N<5>
91 11 6	MEM B DQS P<5>	==	=MEM B DQS P<5>
91 11 6	MEM B DQ<47>	==	=MEM B DQ<47>
91 11 6	MEM B DQ<46>	==	=MEM B DQ<46>
91 11 6	MEM B DQ<45>	==	=MEM B DQ<45>
91 11 6	MEM B DQ<44>	==	=MEM B DQ<44>
91 11 6	MEM B DQ<43>	==	=MEM B DQ<43>
91 11 6	MEM B DQ<42>	==	=MEM B DQ<42>
91 11 6	MEM B DQ<41>	==	=MEM B DQ<41>
91 11 6	MEM B DQ<40>	==	=MEM B DQ<40>
CPU CHANNEL B DQS 6 -> DIMM B DQS 6			
91 11 6	MEM B DQS N<6>	==	MEM B DQS N<6>
91 11 6	MEM B DQS P<6>	==	MEM B DQS P<6>
91 11 6	MEM B DQ<55>	==	=MEM B DQ<55>
91 11 6	MEM B DQ<54>	==	=MEM B DQ<54>
91 11 6	MEM B DQ<53>	==	=MEM B DQ<53>
91 11 6	MEM B DQ<52>	==	=MEM B DQ<52>
91 11 6	MEM B DQ<51>	==	=MEM B DQ<51>
91 11 6	MEM B DQ<50>	==	=MEM B DQ<50>
91 11 6	MEM B DQ<49>	==	=MEM B DQ<49>
91 11 6	MEM B DQ<48>	==	=MEM B DQ<48>
CPU CHANNEL B DQS 7 -> DIMM B DQS 7			
91 11 6	MEM B DQS N<7>	==	=MEM B DQS N<7>
91 11 6	MEM B DQS P<7>	==	=MEM B DQS P<7>
91 11 6	MEM B DQ<63>	==	=MEM B DQ<63>
91 11 6	MEM B DQ<62>	==	=MEM B DQ<62>
91 11 6	MEM B DQ<61>	==	=MEM B DQ<61>
91 11 6	MEM B DQ<60>	==	=MEM B DQ<60>
91 11 6	MEM B DQ<59>	==	=MEM B DQ<59>
91 11 6	MEM B DQ<58>	==	=MEM B DQ<58>
91 11 6	MEM B DQ<57>	==	=MEM B DQ<57>
91 11 6	MEM B DQ<56>	==	=MEM B DQ<56>

D

C

B

A

SYNC MASTER=K92 SUMA		SYNC DATE=05/10/2010	
PAGE TITLE		PAGE	
DDR3 Byte/Bit Swaps		DRAWING NUMBER	SIZE
 Apple Inc.		REVISION	D
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		PAGE	30 OF 132
		SHEET	27 OF 101

Page Notes

Power aliases required by this page:

- =PP1V5_S0_MEM_B
- =PP1V5_S3_MEM_B
- =PP0V75_S0_MEM_VTT_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

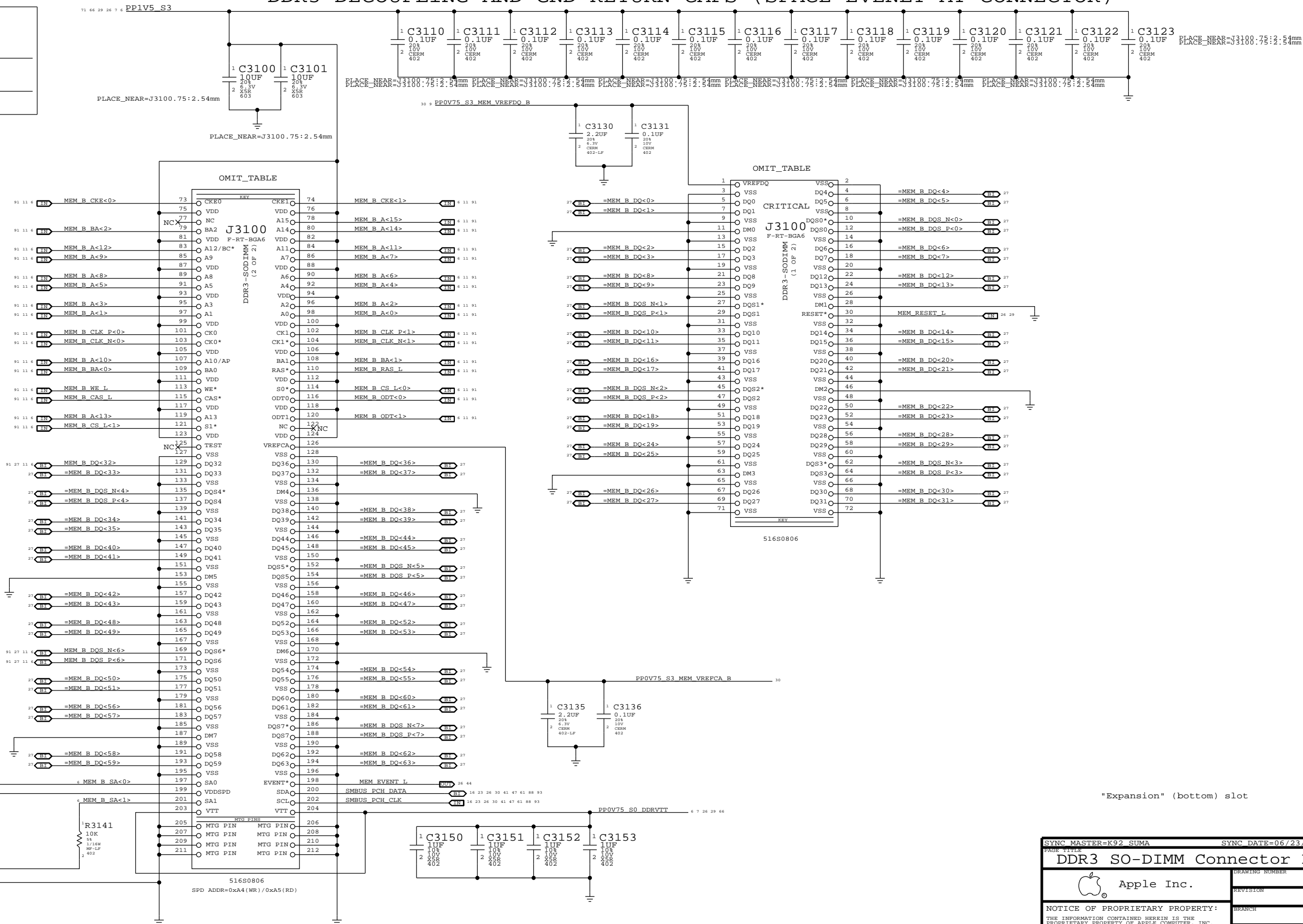
Signal aliases required by this page:

- =I2C_S0DIMM_SCL
- =I2C_S0DIMM_SDA

BOM options provided by this page:

(NONE)

DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)



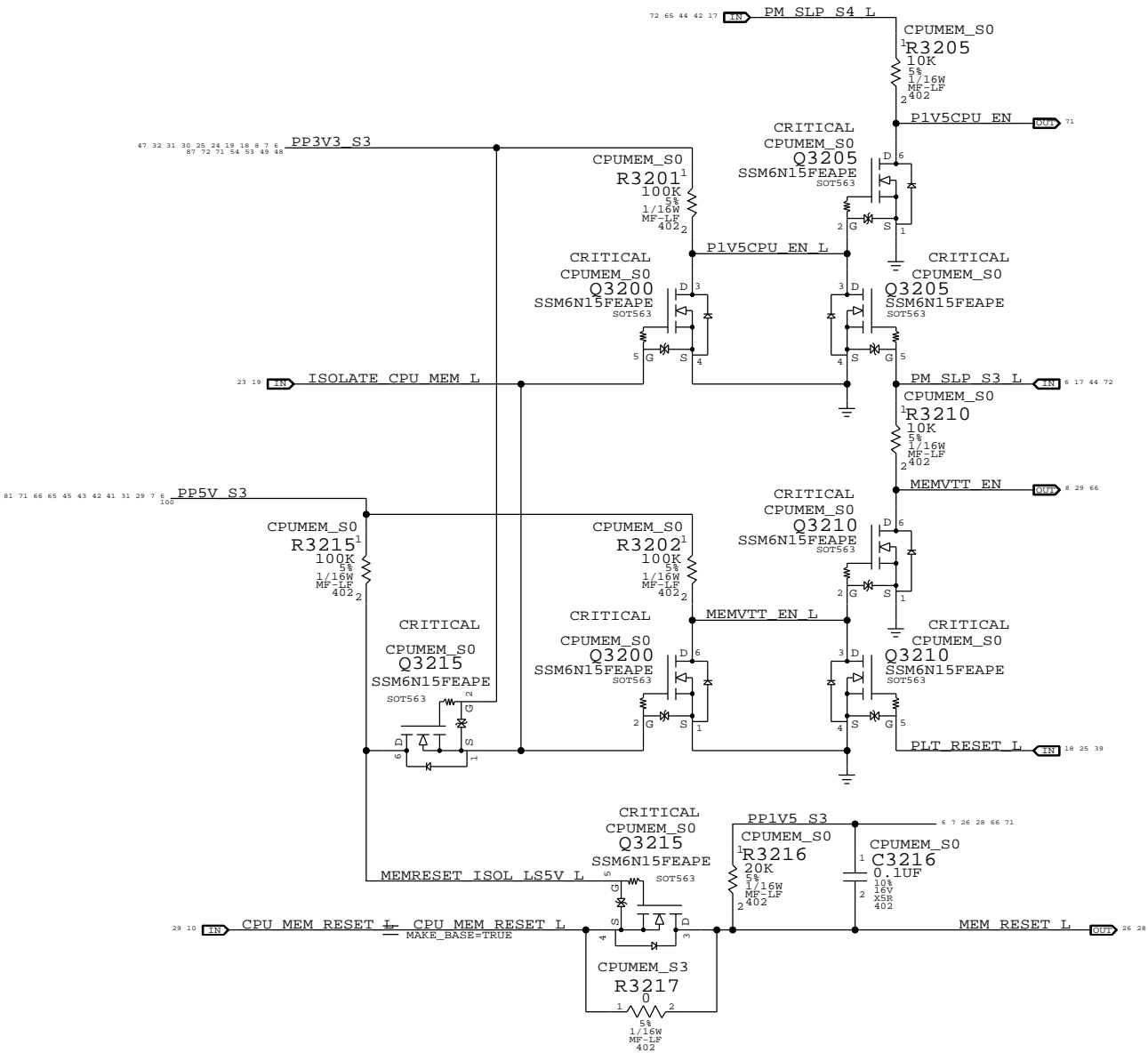
"Expansion" (bottom) slot

SYNC_MASTER=K92_SUMA		SYNC_DATE=06/23/2010	
PAGE TITLE			
DDR3 SO-DIMM Connector B			
Apple Inc.		DRAWING NUMBER	SIZE
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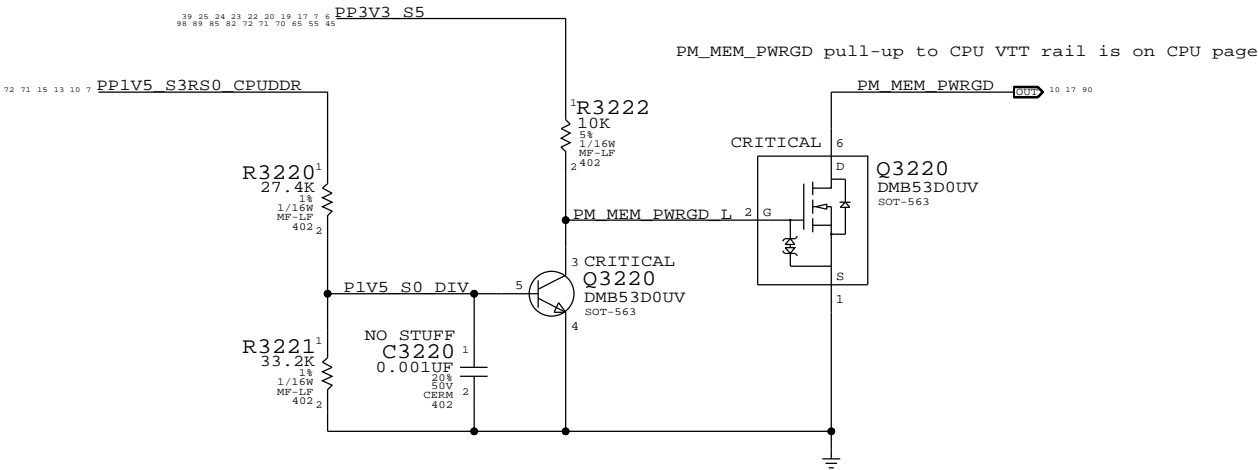
The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3->S0 transitions determines behavior of signals.
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

P1V5CPU_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L
MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L

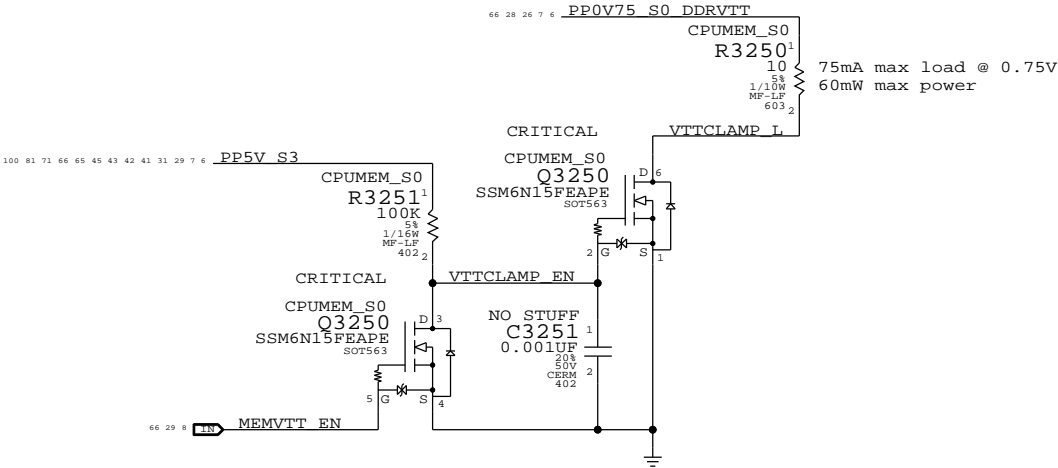


1V5 S0 "PGOOD" for CPU



MEMVTT Clamp

Ensures CKE signals are held low in S3



Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	P1V5CPU_EN
S0	0	1	1	1	1	CPU_MEM_RESET_L	1	1
to	1	0	1	1	1	1	1	1
2	0	0	1	1	1	1	0	1
3	0	0	0	1	X	1	0	0
4	0	0	1	1	X	1	0	1
5	0	1	1	1	0 (*)	1	1	1
6	0	1	1	1	1	1	1	1
S0	7	1	1	1	1	CPU_MEM_RESET_L	1	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

SYNC MASTER=K18 MLB

SYNC DATE=04/27/2010

CPU Memory S3 Support

Apple Inc.

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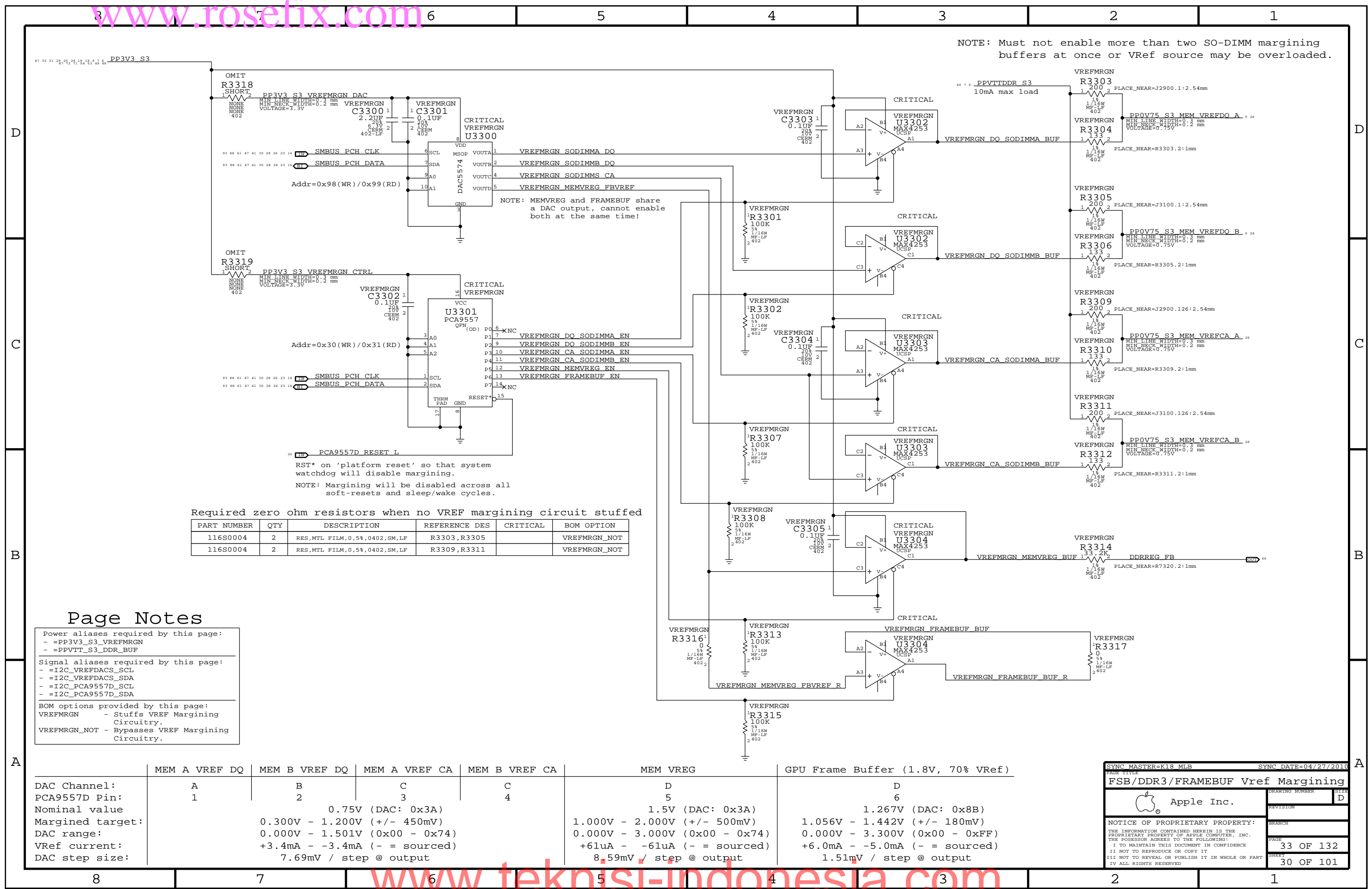
BRANCH

PAGE

SHEET

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Page Notes

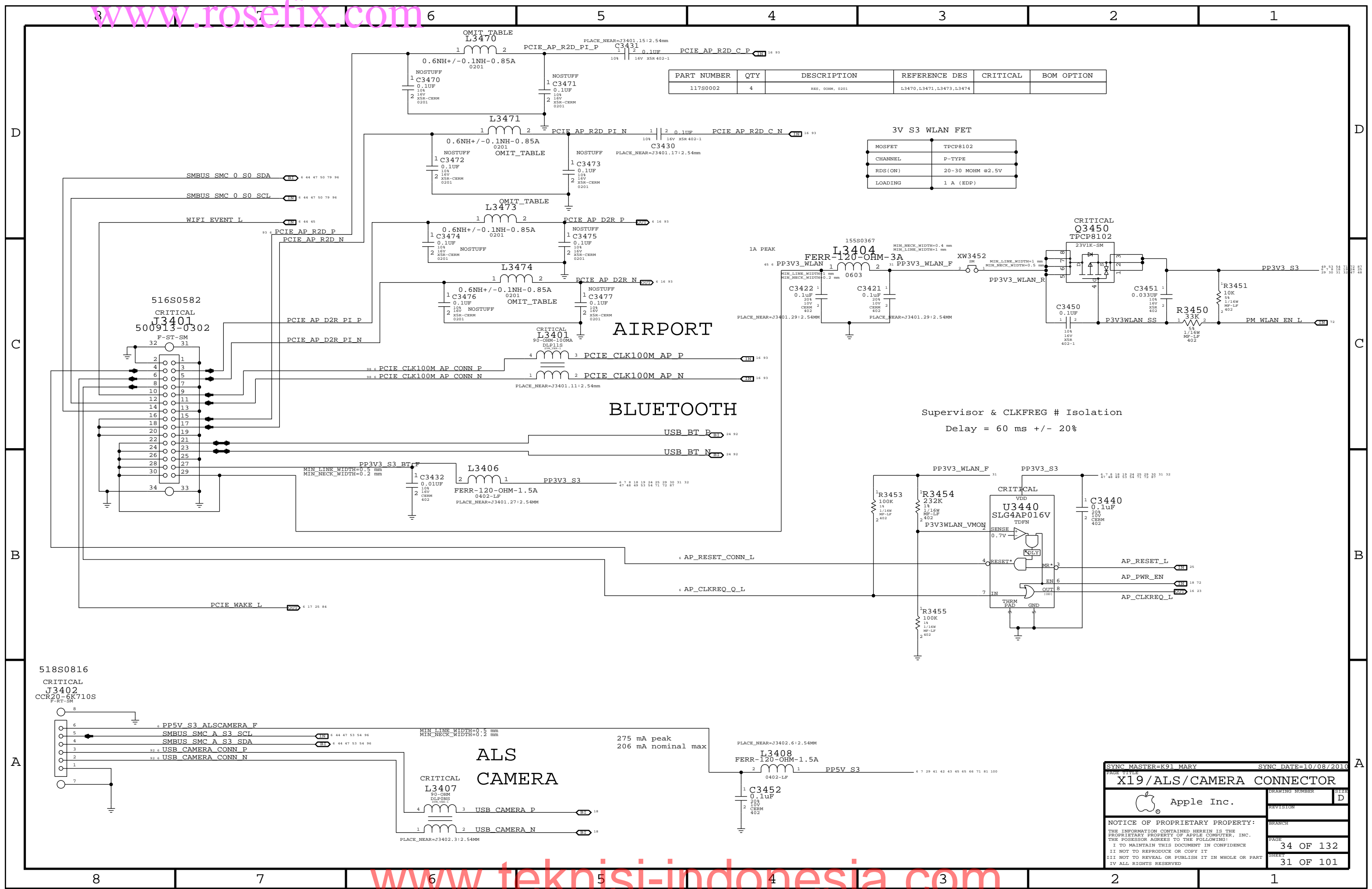
Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN - Stuffs VREF Margining Circuitry.
VREFMRGN_NOT - Bypasses VREF Margining Circuitry.

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% Vref)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	6
Nominal value			0.75V (DAC: 0x3A)		1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:			0.300V - 1.200V (+/- 450mV)		1.000V - 2.000V (+/- 500mV)	1.056V - 1.442V (+/- 180mV)
DAC range:			0.000V - 1.501V (0x00 - 0x74)		0.000V - 3.000V (0x00 - 0x74)	0.000V - 3.300V (0x00 - 0xFF)
Vref current:			+3.4mA - -3.4mA (- = sourced)		+61uA - -61uA (- = sourced)	+6.0mA - -5.0mA (- = sourced)
DAC step size:			7.69mV / step @ output		8.59mV / step @ output	1.51mV / step @ output

SYNC MASTER=K18 MLB		SYNC DATE=04/27/2010	
PAGE TITLE		FSB/DDR3/FRAMEBUF Vref Margining	
DRAWING NUMBER		SIZE	
Apple Inc.		D	
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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0002	4	RES, 008M, 0201	L3470,L3471,L3473,L3474		

3V S3 WLAN FET	
MOSFET	TPCP8102
CHANNEL	P-TYPE
RDS(ON)	20-30 MOHM @2.5V
LOADING	1 A (EDP)

AIRPORT

BLUETOOTH


Supervisor & CLKFREG # Isolation
Delay = 60 ms +/- 20%

518S0816

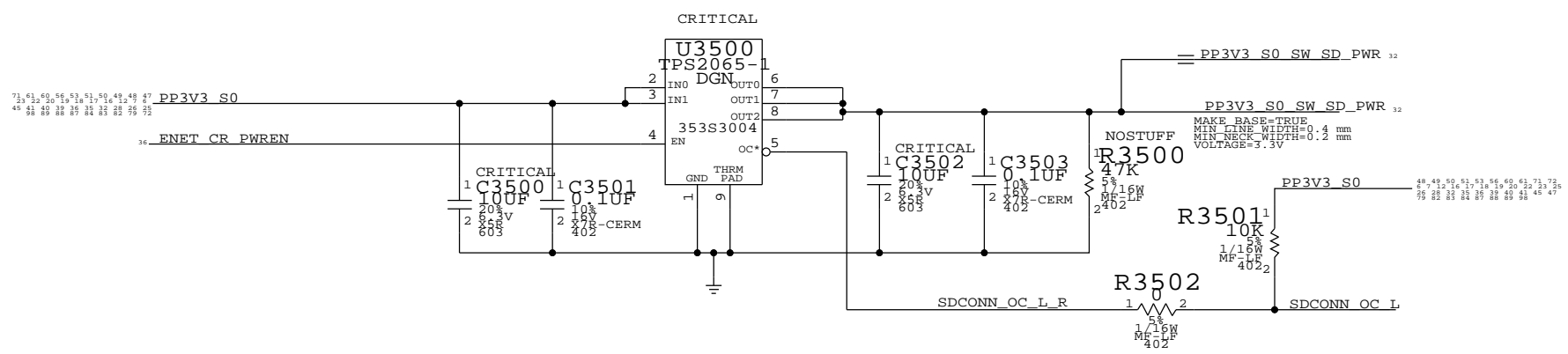
CRITICAL
J3402
CCR20-6K710S

ALS
CAMERA

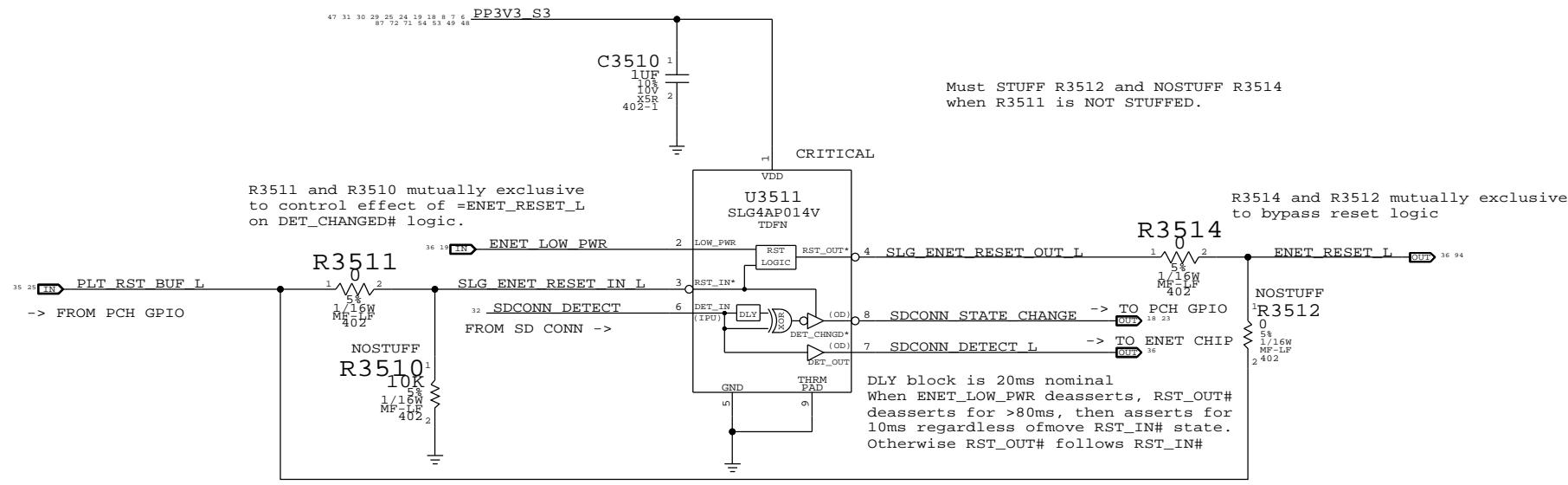
275 mA peak
206 mA nominal max

SYNC MASTER=K91 MARY		SYNC DATE=10/08/2010	
PAGE TITLE			
X19/ALS/CAMERA CONNECTOR			
 Apple Inc.		DRAWING NUMBER	SIZE
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		PAGE	34 OF 132
		SHEET	31 OF 101

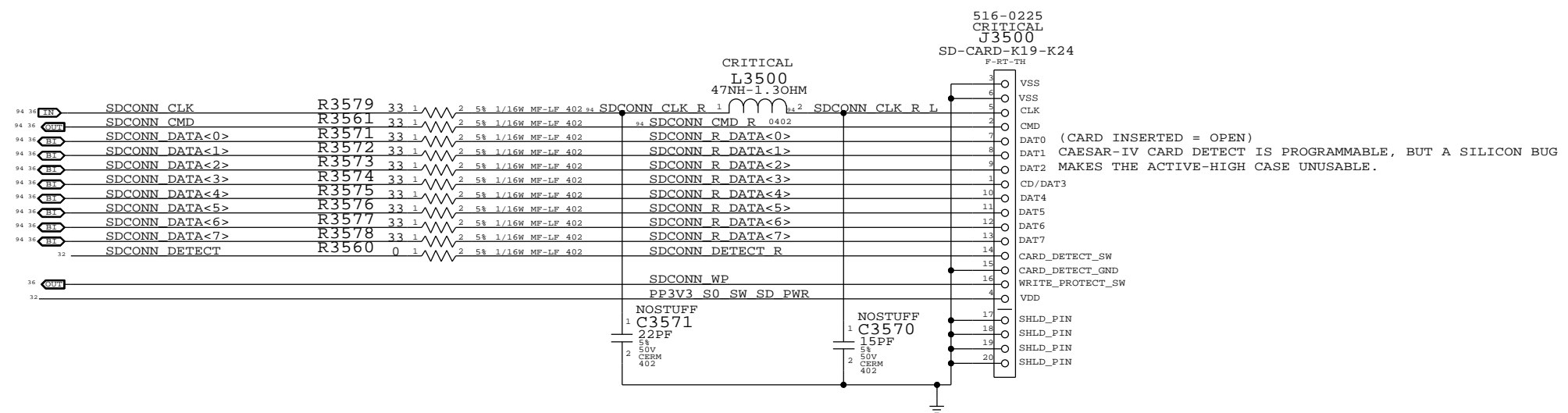
SD CARD 3.3V OVERCURRENT PROTECTION CHIP WITH ACTIVE LOAD DISCHARGE



SDCONN DETECT DEBOUNCE, INVERSION, AND DETECT-CHANGED PCH GPIO LATCH CIRCUIT



SD CARD CONNECTOR



SD READER CONNECTOR

Apple Inc.

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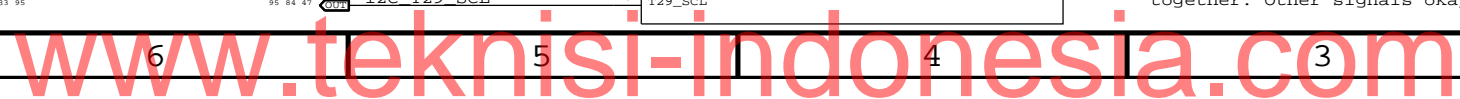
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REVISION: 32 OF 101





Page Notes

Power aliases required by this page:

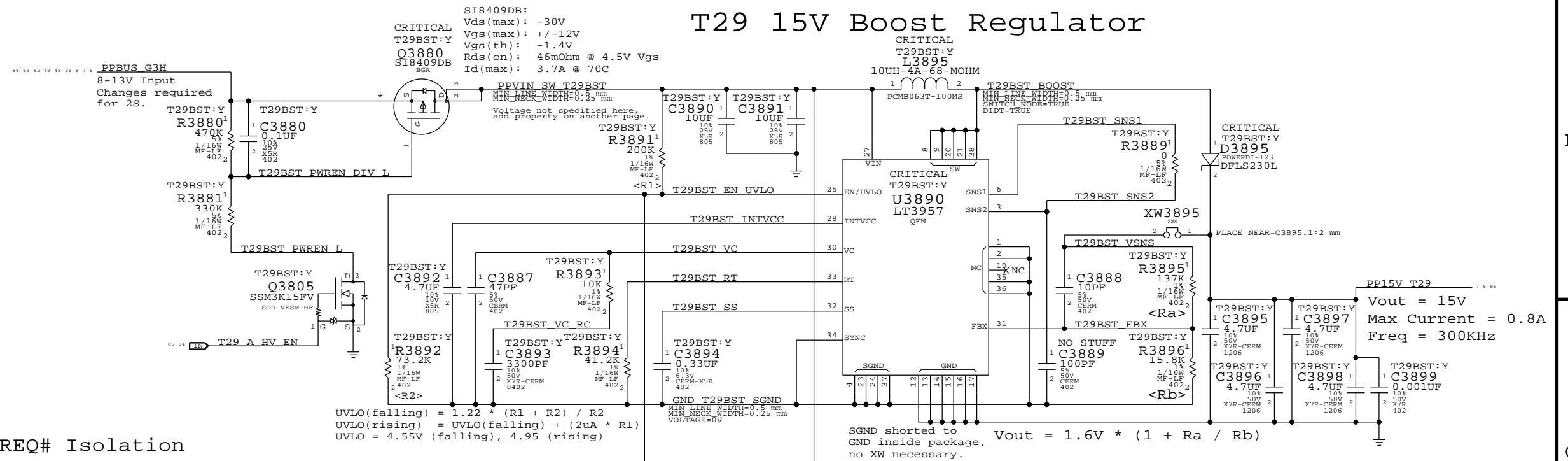
- ```
- =PPVIN_SW_T29RST (8-13V Boost Input)
- =PP18V_T29_REG (18V Boost Output)
- =PP3V3_T29_P3V3T29FET (3.3V FET Input)
- =PP3V3_T29_FET (3.3V FET Output)
- =PP3V3_S0_T29PWRCTL
- =PPIV05_T29_PIV05T29FET (1.05V FET Input)
- =PPIV05_T29_FET (1.05V FET Output)
```

Signal aliases required by this page:

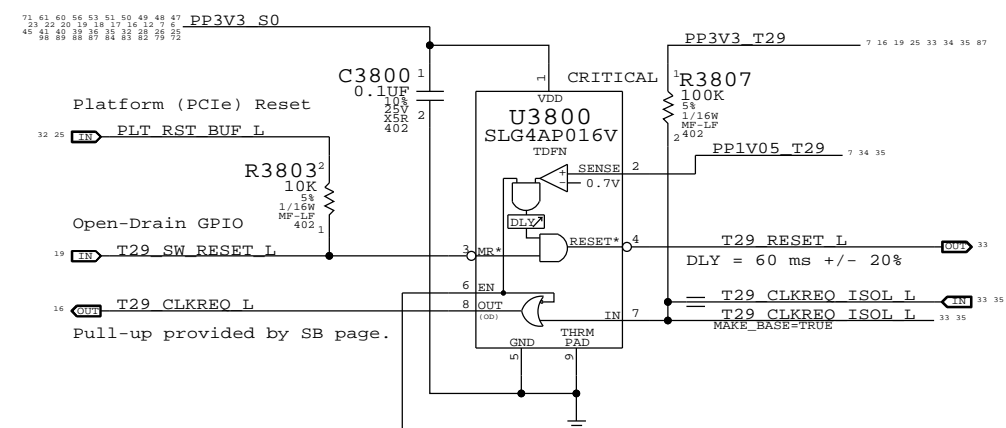
- ```
- =T29_CLKREQ_L
- =T29_RESET_L
```

BOM options provided by this page:

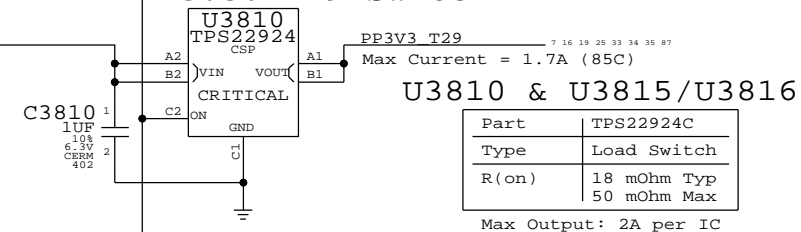
T29BST:Y - Stuffs 18V boost circuitry.



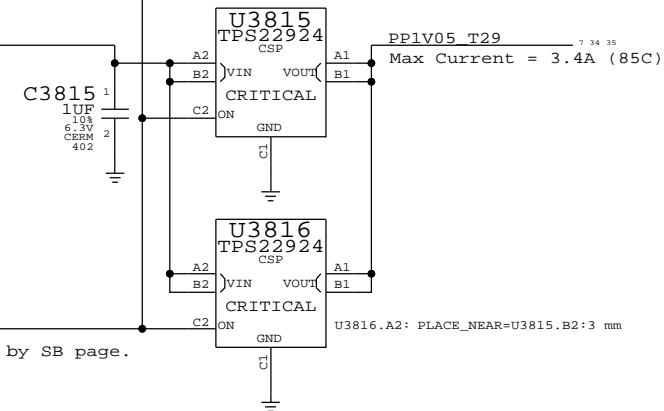
Supervisor & CLKREQ# Isolation



3.3V T29 Switch




1.05V T29 Switch

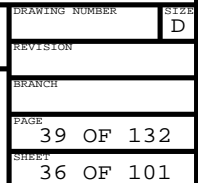


Part	TPS22924C
Type	Load Switch
R(on)	18 mOhm Typ 50 mOhm Max

Max Output: 2A per IC

SYNCH MASTER-T29 REF		SYNCH DATE=10/12/2010	
PAGE TITLE			
T29 Power Support			
 Apple Inc.		DRAWING NUMBER	
		SIZE	
		D	
		REVISION	
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```
PP1V2 ENET 6 7 36 70
???mA (1000base-T, Caesar V)
```

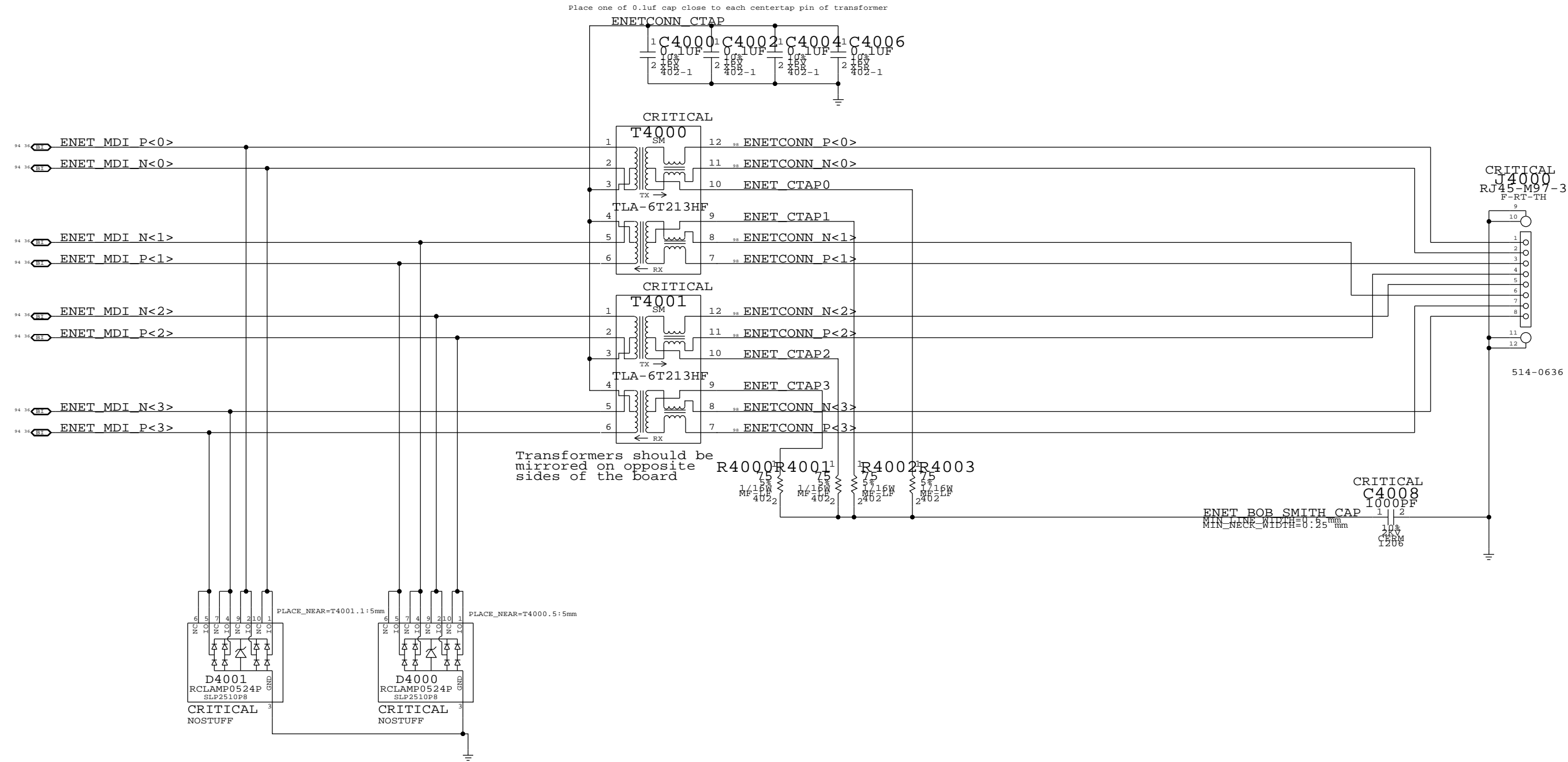


Page Notes

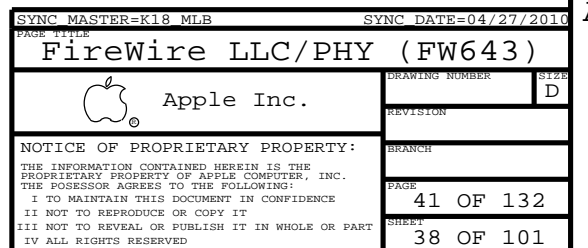
Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



PAGE TITLE		PAGE	
Ethernet Connector		40 OF 132	
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Page Notes

Power aliases required by this page:

- =PPBUS_S5_FWPWRSW (FW VP FET Input)
- =PPBUS_FW_FET (FW VP FET Output)
- =PP3V3_FW_P3V3FWFET (3.3V FET Input)
- =PP3V3_FW_FET (3.3V FET Output)
- =PP3V3_FW_FWPHY (PHY 3.3V Power)
- =PP3V3_S0_FWLATEVG
- =PP3V3_S0_FWPWRCTL (5KPD Bias Rail)
- =PP1V05_S0_FWPWRCTL (5KPD Bias Rail)
- =PP1V05_FW_P1V0FWFET (1.0V FET Input)
- =PP1V0_FW_FET_R (1.0V FET Output)
- =PP1V0_FW_FWPHY (PHY 1.0V)

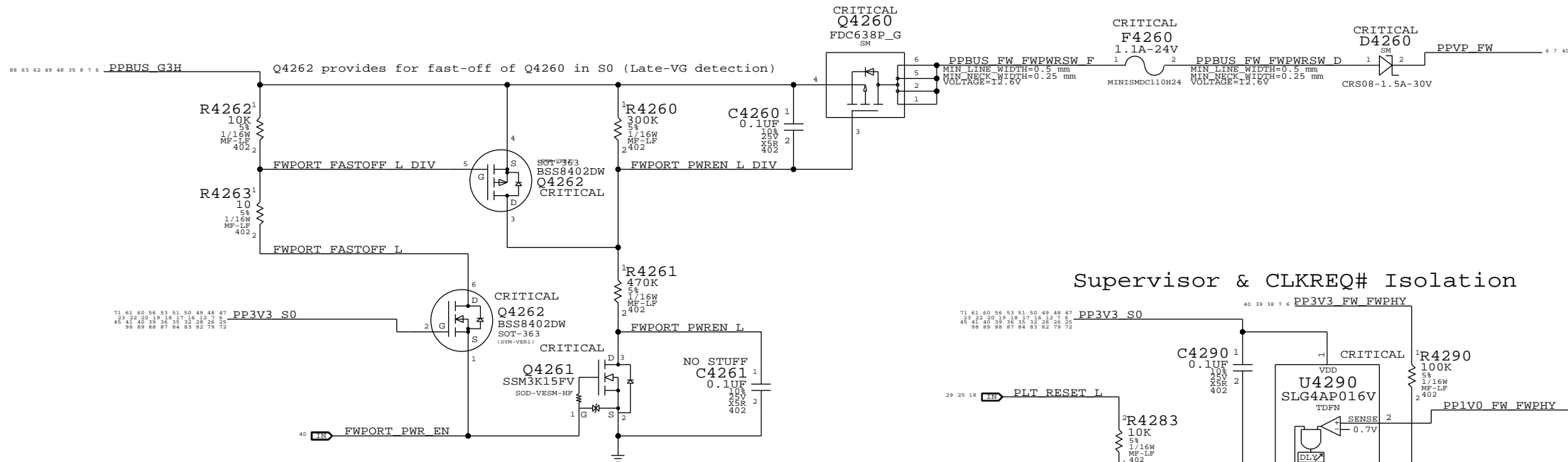
Signal aliases required by this page:

- =FW_CLKREQ_L
- =FW_PME_L

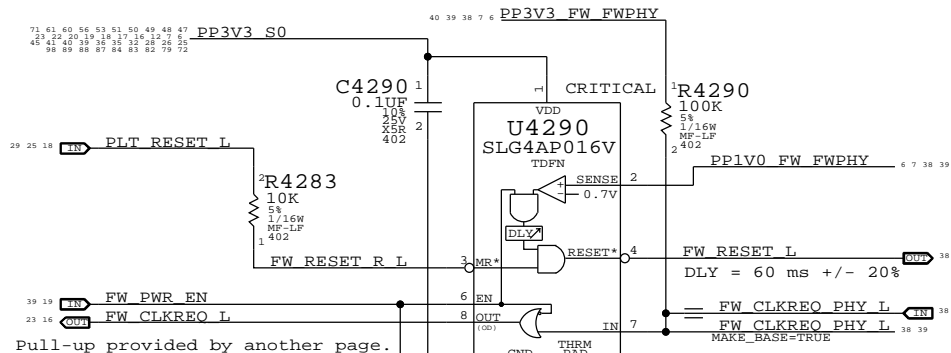
BOM options provided by this page:

(NONE)

FireWire Port Power Switch

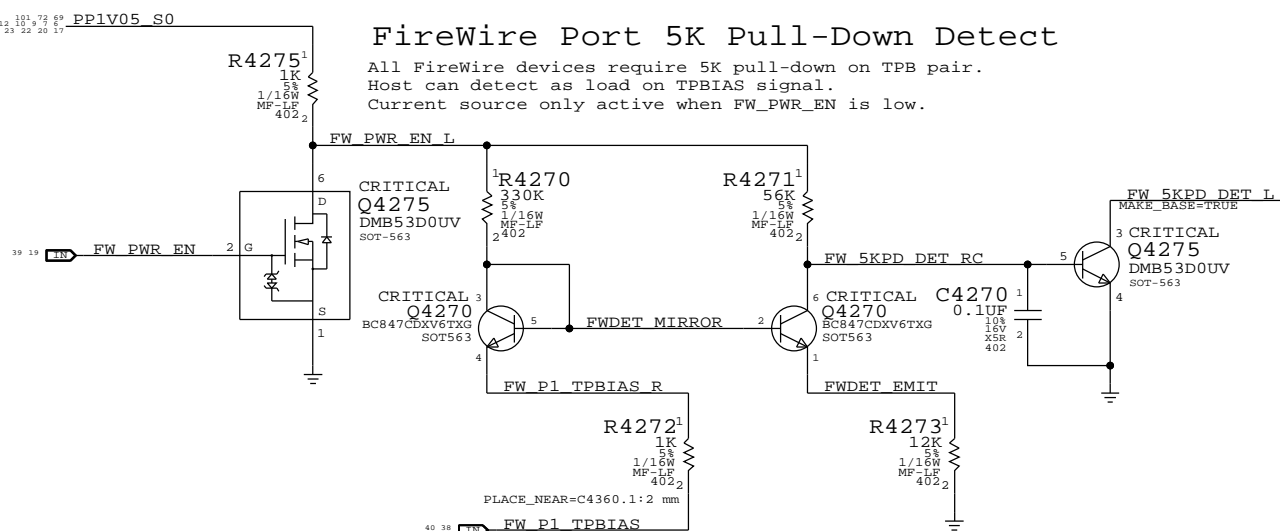


Supervisor & CLKREQ# Isolation



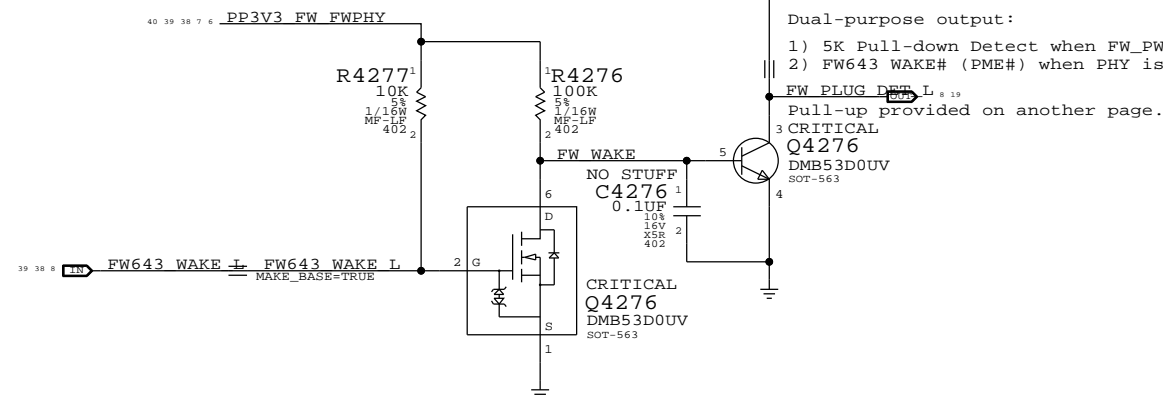
FireWire Port 5K Pull-Down Detect

All FireWire devices require 5K pull-down on TPB pair.
Host can detect as load on TPBIAS signal.
Current source only active when FW_PWR_EN is low.



FireWire PHY WAKE# Support

When PHY is powered, FW_5KPD_DET_L acts as legacy PME# signal.

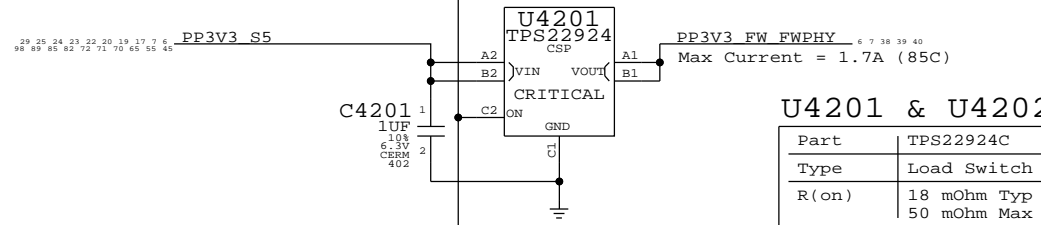


Dual-purpose output:

- 1) 5K Pull-down Detect when FW_PWR_EN is low.
- 2) FW643 WAKE# (PME#) when PHY is powered.

Pull-up provided on another page.

3.3V FW Switch

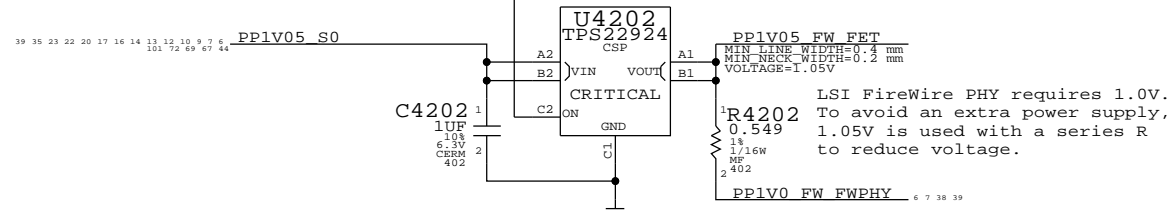


U4201 & U4202

Part	TPS22924C
Type	Load Switch
R(on)	18 mOhm Typ 50 mOhm Max

Max Output: 2A

1.0V FW Switch



SYNC MASTER=T27 REF		SYNC DATE=06/10/2010	
PAGE TITLE		FireWire Port & PHY Power	
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Page Notes

Power aliases required by this page:
- =PPVP_FW_PORT1
- =PPVP_FW_PHY_CPS_FET (From Port)
- =PPVP_FW_PHY_CPS (To PHY)
- =PP3V3_FW_FWPHY
- =PP3V3_S0_FWLATEVG

Signal aliases required by this page:
- =FW_PHY_DS0
- =FW_PHY_DS1
- =FW_PHY_DS2

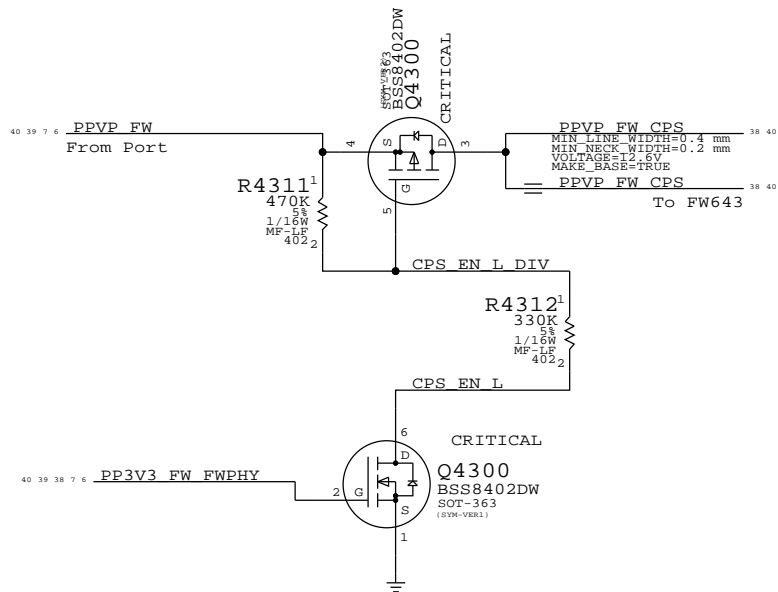
NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:
(NONE)

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

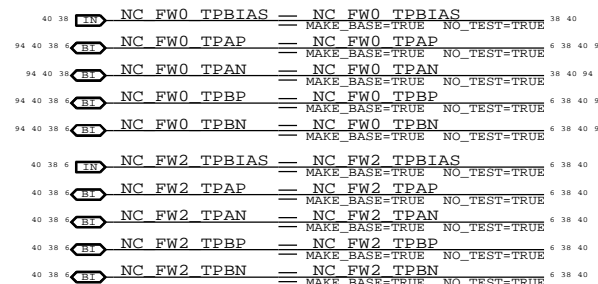
FW643 TPCPS Leakage Protection

FW643 has internal leakage path from TPCPS pin to VDD33.
FET blocks current to TPCPS until VDD33 is powered.



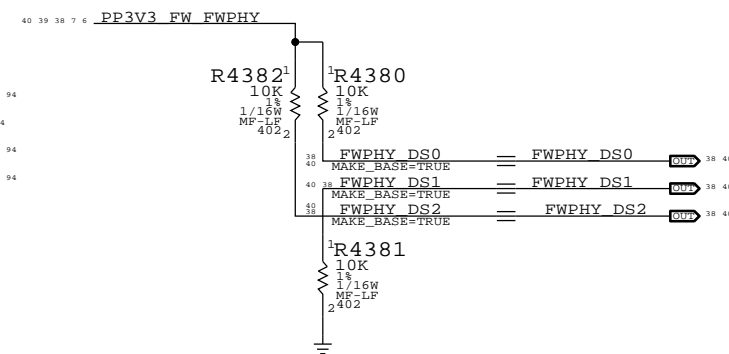
Unused FireWire Ports

Disabled per LSI instructions
(All unused port signals TP/NC)



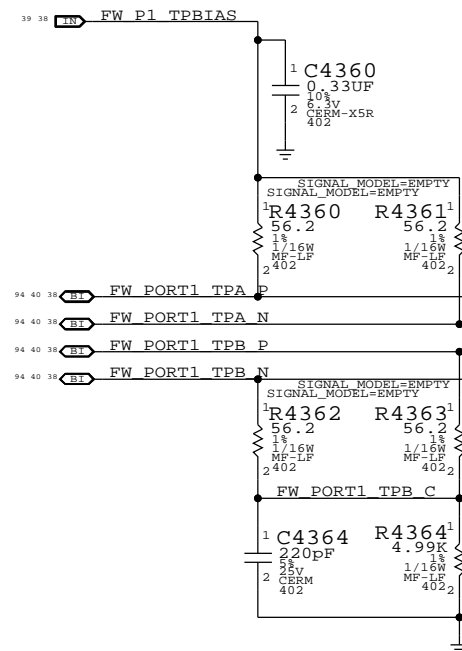
FireWire PHY Config Straps

Configures PHY for:
- Port "1" Bilingual (1394B)



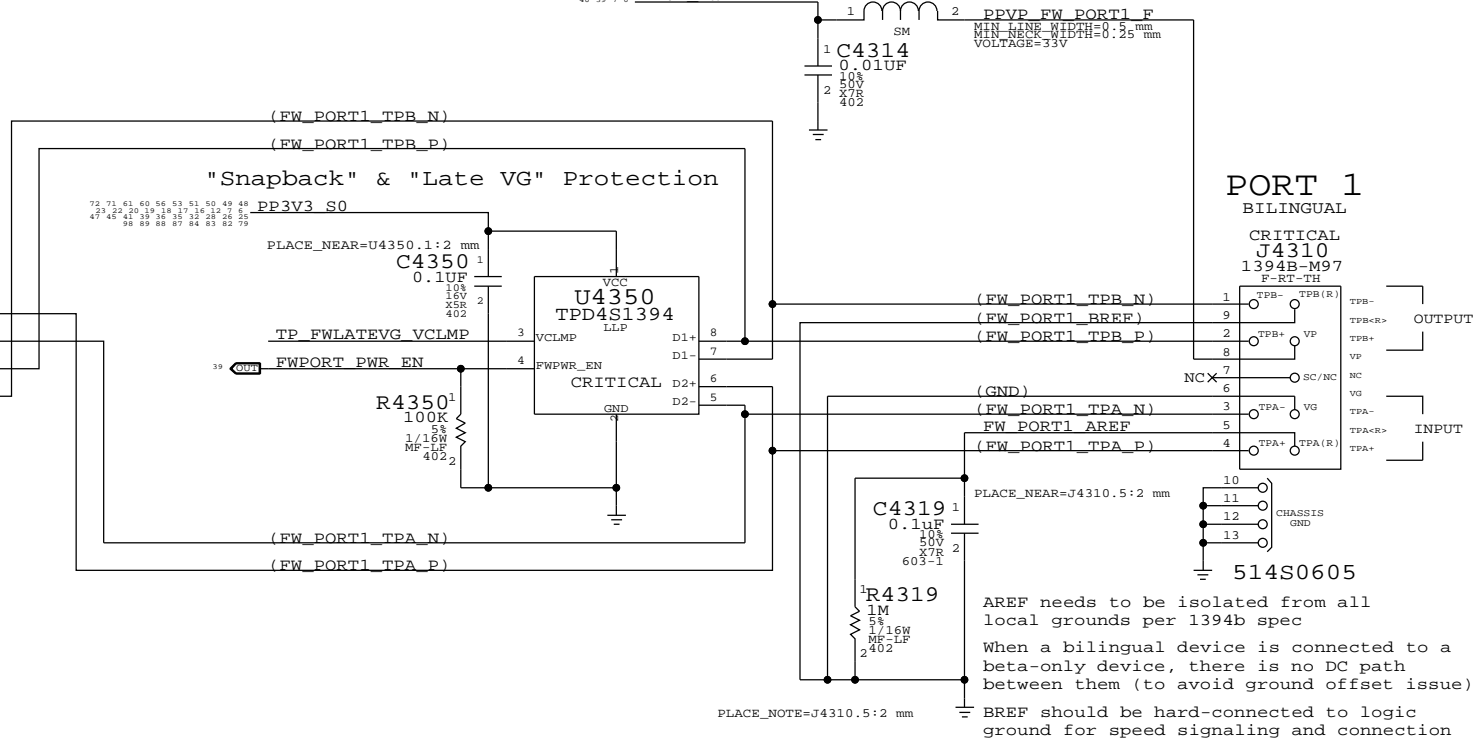
Termination

Place close to FireWire PHY



Cable Power

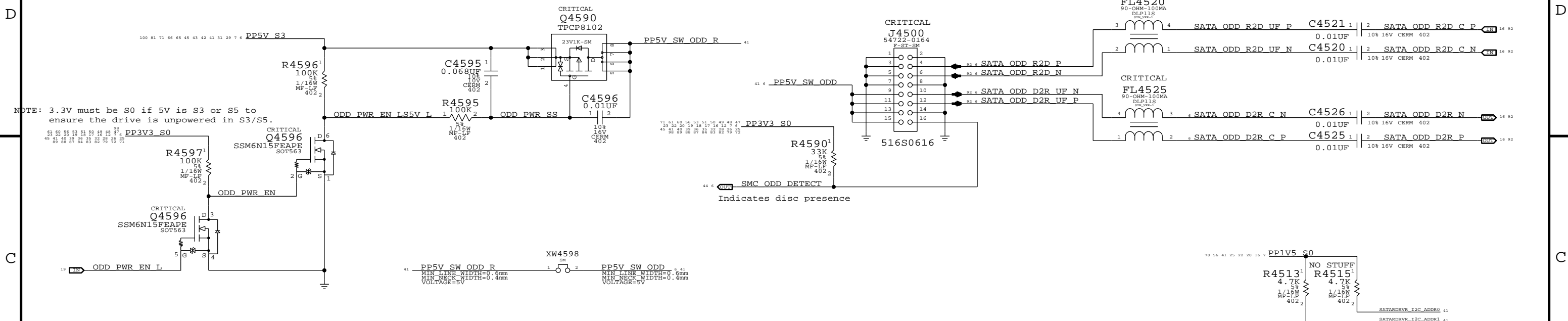
CRITICAL L4310 FERR-250-OHM Note: Trace PPVP_FW_PORT1 must handle up to 5A



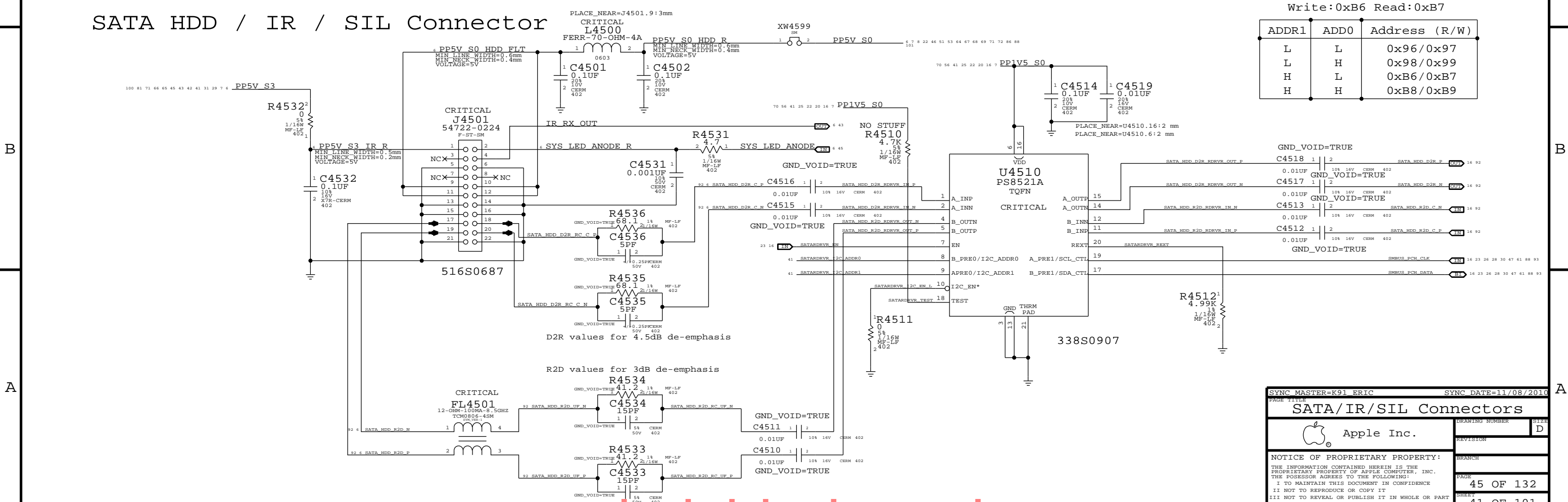
SYNC MASTER=T27 REF		SYNC DATE=06/10/2010	
PAGE TITLE			
FireWire Connector		DRAWING NUMBER	SIZE
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SATA ODD Connector

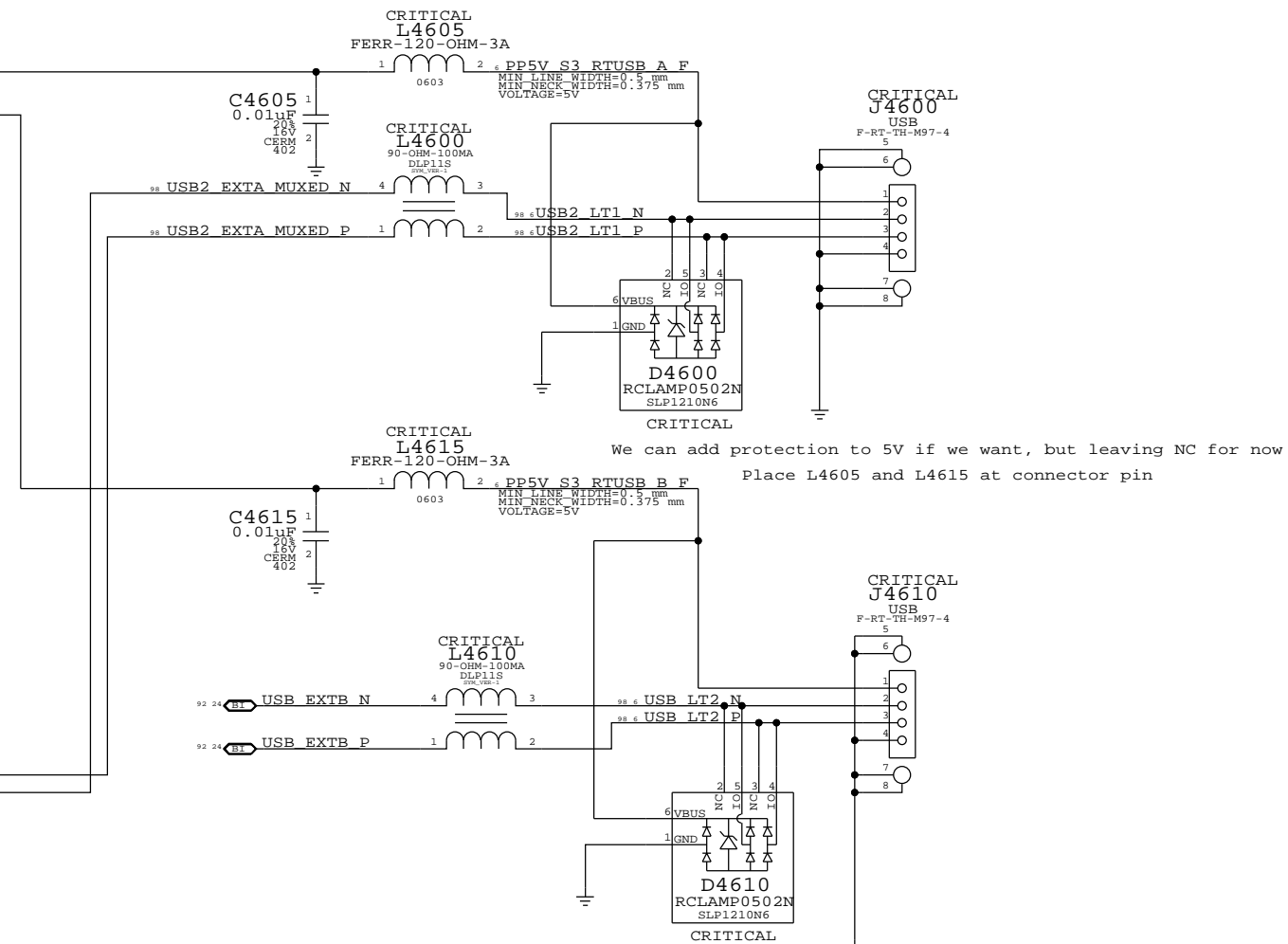
ODD Power Control



SATA HDD / IR / SIL Connector



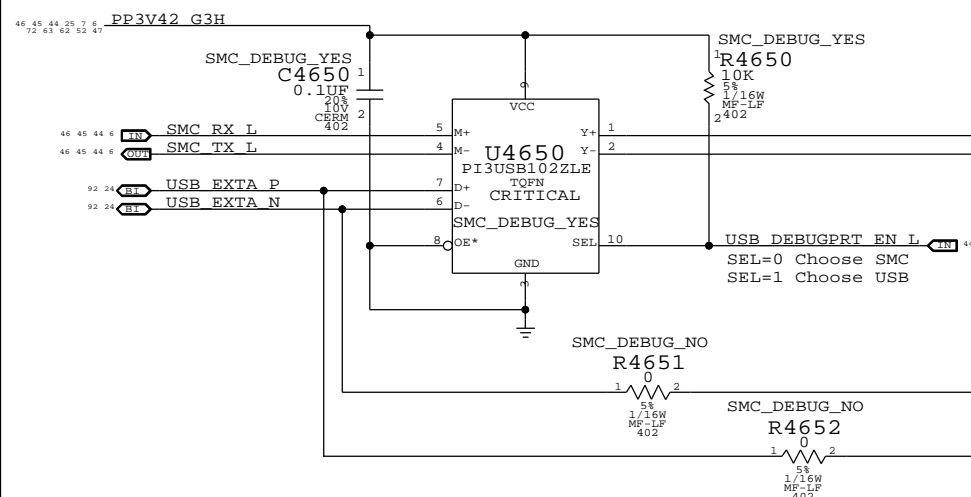
Left USB Port A




We can add protection to 5V if we want, but leaving NC for now

Place L4605 and L4615 at connector pin

Left USB Port B



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PAGE			
External USB Connectors			
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NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.

D

D

C

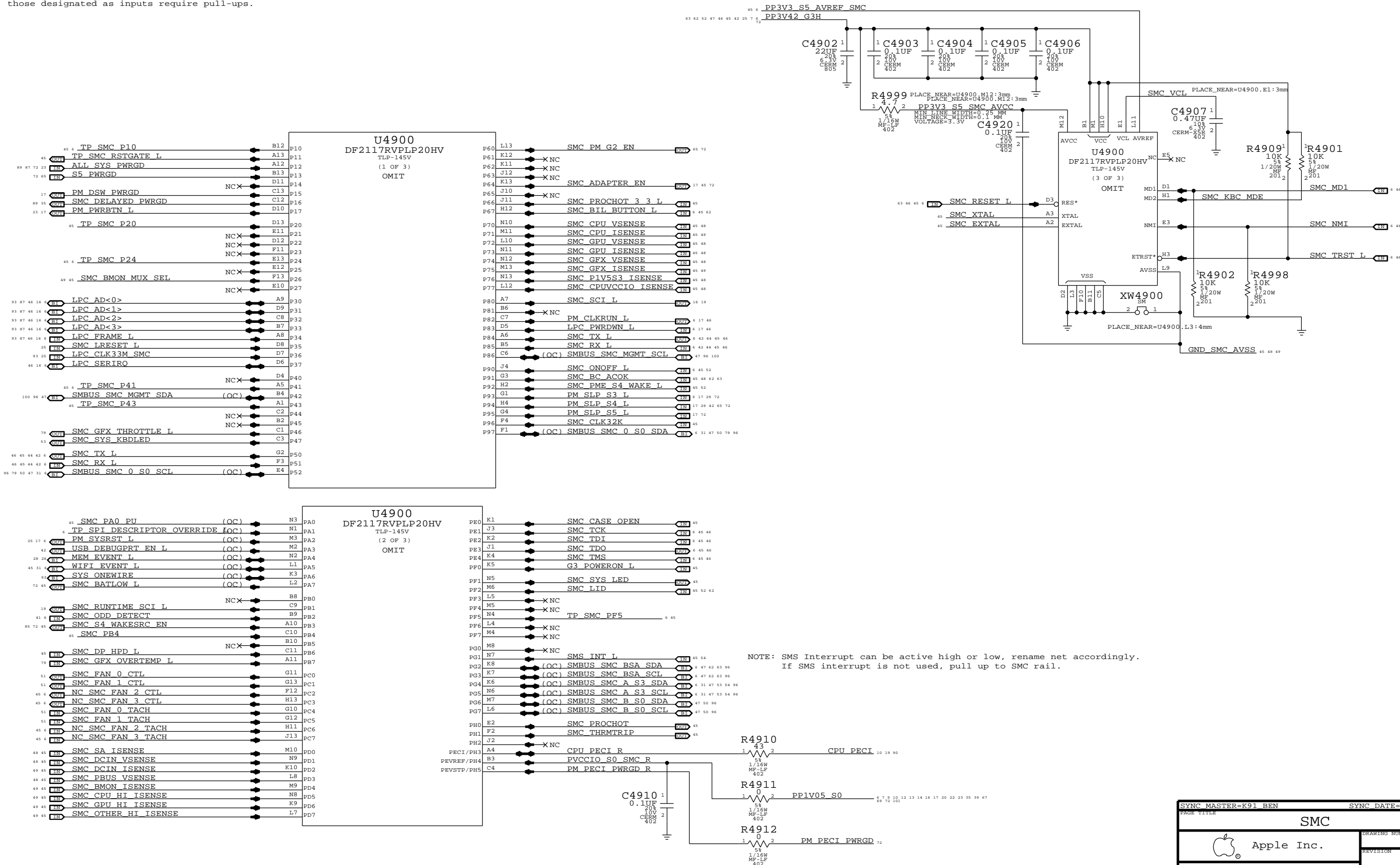
C

B

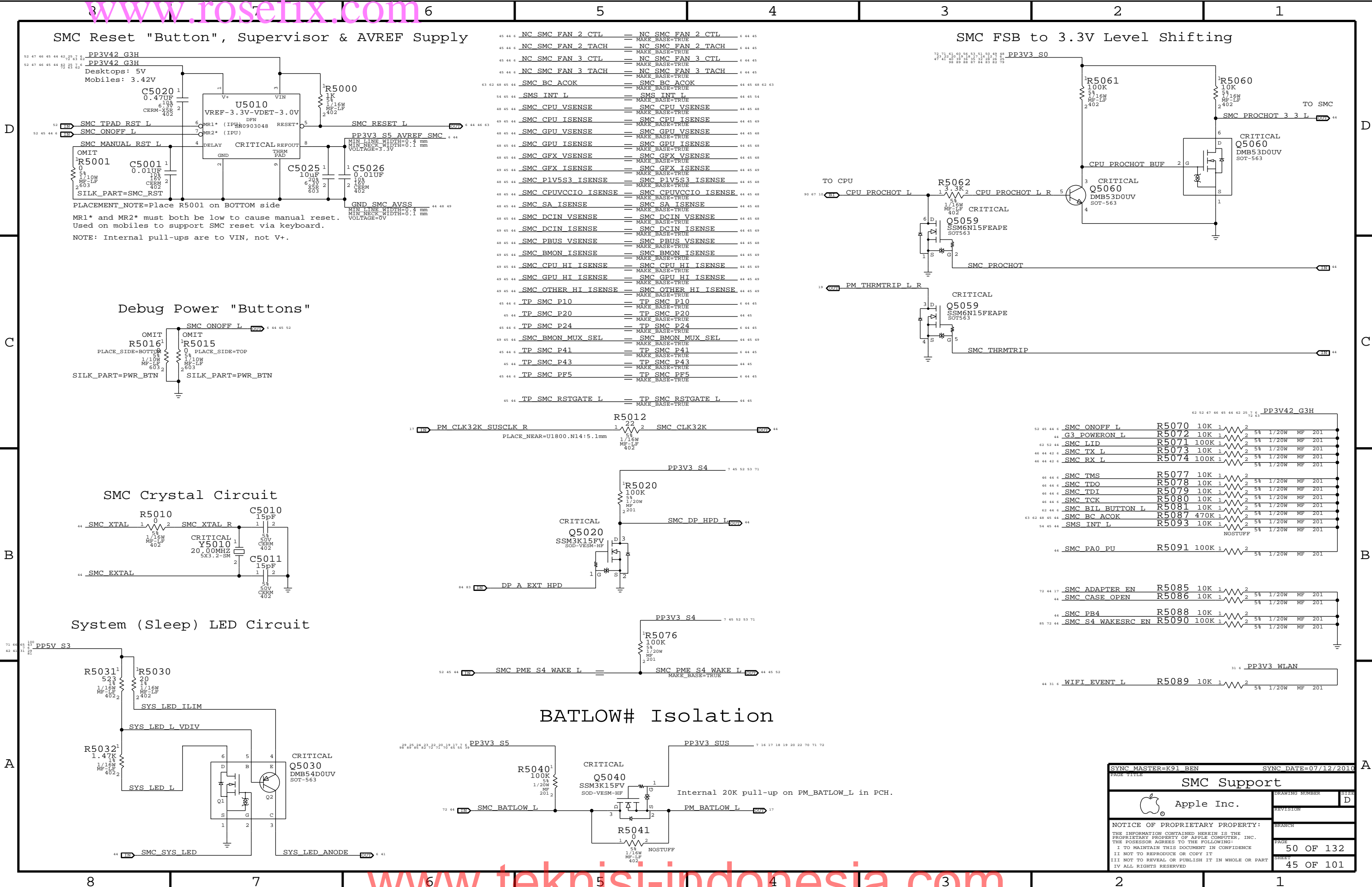
B

A

A



SYNC MASTER=K91 BEN		SYNC DATE=07/12/2010	
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		DRAWING NUMBER	SIZE
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SYNC DATE=07/12/2010

SMC Support

Apple Inc.

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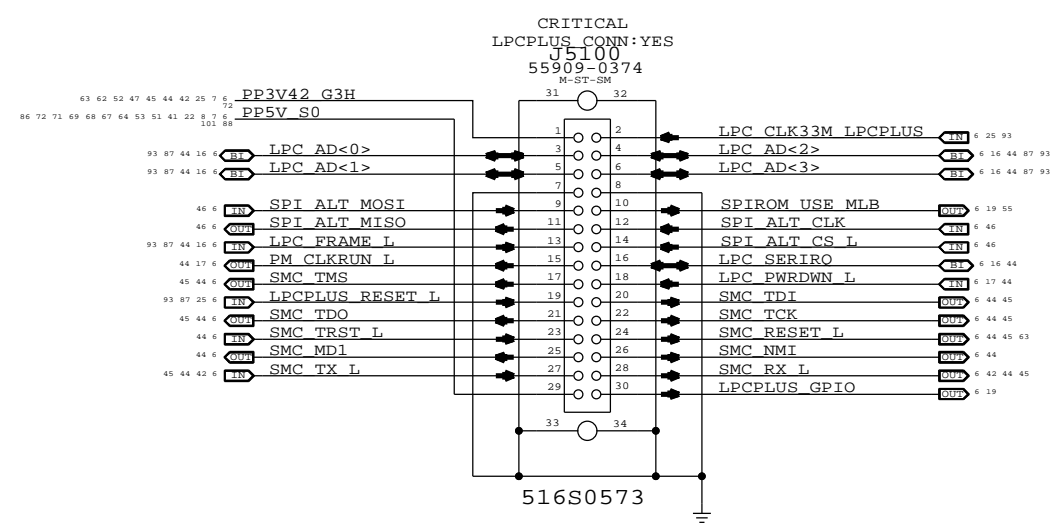
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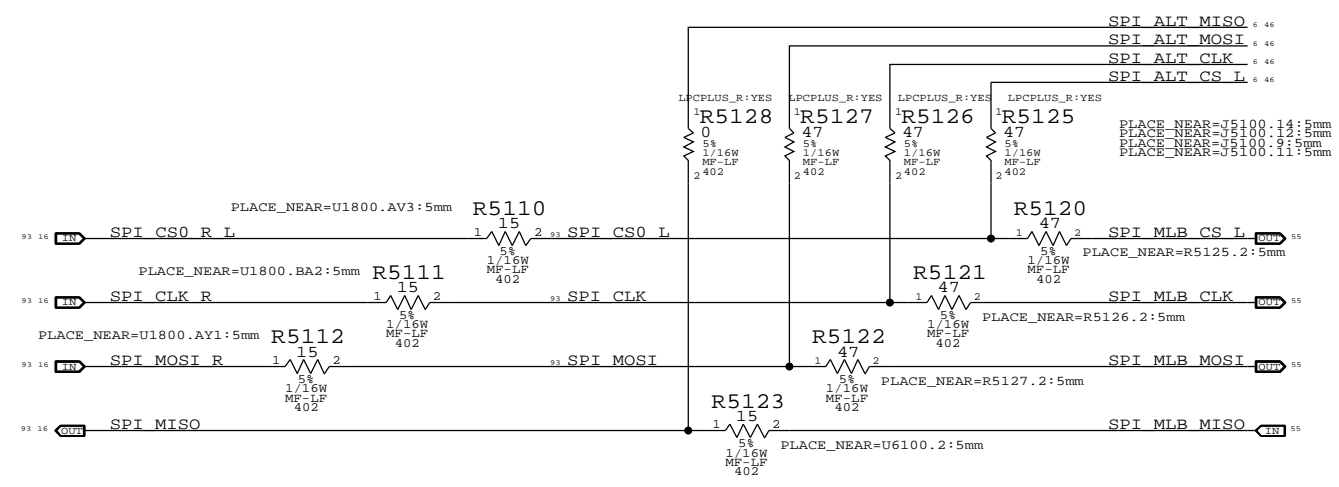
50 OF 132

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LPC+SPI Connector



SPI Bus Series Termination





D



C



B



A



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0090	4	RES, 00HM, 0402	C5308,C5327,C5367,C5377		ISNS_ON:NO

EDP:18A

Vi=Voltage across R7350=0.006V=0.018V ISNS_ON:YES

CRITICAL

U5360

OPA2333

PLACE_NEAR=U4900.N13:5mm

SMC Key IMOC

SMC_ADC6

R5373

5.49K

ISNS_1V5_S3_P

ISNS_1V5_S3_R_P

R5374

5.49K

ISNS_1V5_S3_N

ISNS_1V5_S3_R_N

R5375

1M

ISNS_ON:YES

R5376

1M

Gain: 182x

ISNS_ON:YES

SIGNAL_MODEL=EMPTY

R5377

4.53K

ISENSE_P1V5S3_IOUT

ISNS_ON:YES


C5377

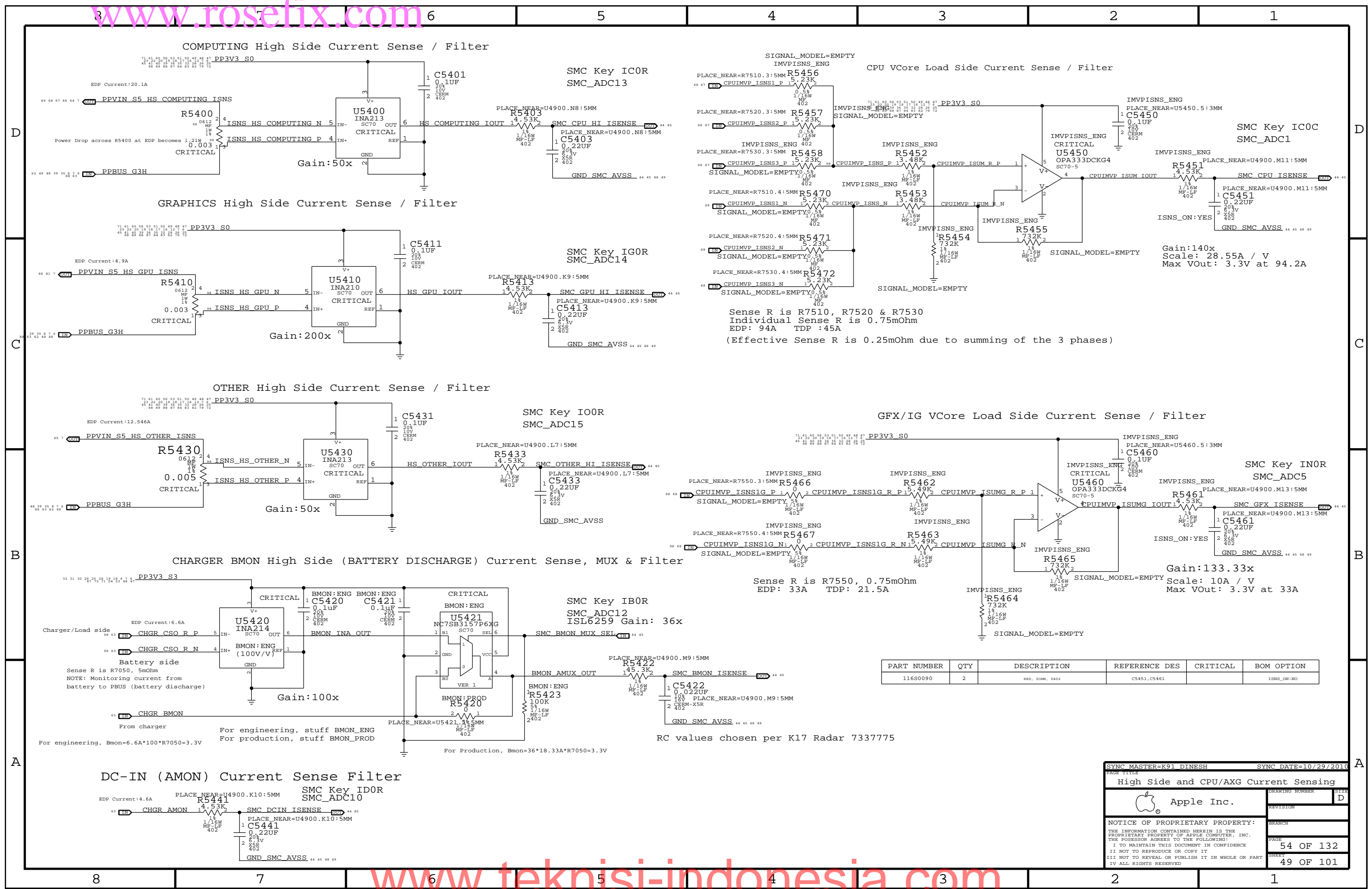
0.22UF

ISNS_ON:YES

SMC_P1V5S3_ISENSE

SMC_AVSS

SYNC MASTER-K91 DINESH		SYNC DATE=08/16/2010	
PAGE TITLE			
Voltage & Load Side Current Sensing			
 Apple Inc.		DRAWING NUMBER	
		SIZE	
		REVISION	
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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0090	2	RES, 00HM, 0402	C5451,C5461		ISNS_ON:NO

SYNC MASTER=K91 DINESH

SYNC DATE=10/29/2010

High Side and CPU/AXG Current Sensing

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SIZE
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D



B



SYNC MASTER=K91 DINESH		SYNC DATE=09/22/2010	
PAGE TITLE			
Thermal Sensors		DRAWING NUMBER	
 Apple Inc.		SIZE	
		D	
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		SHEET 50 OF 101	

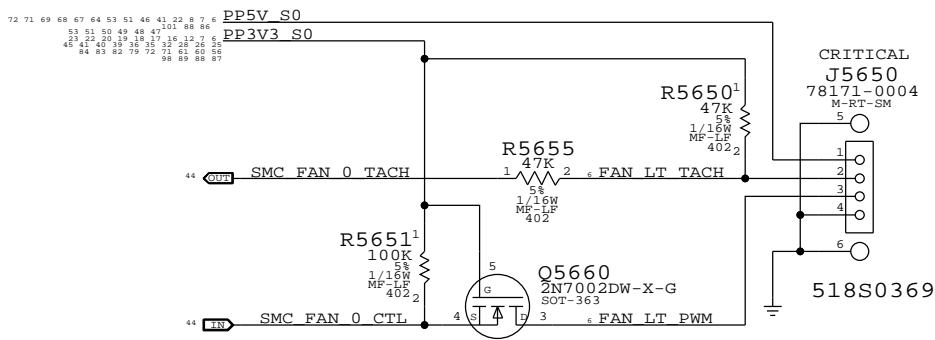
D

C

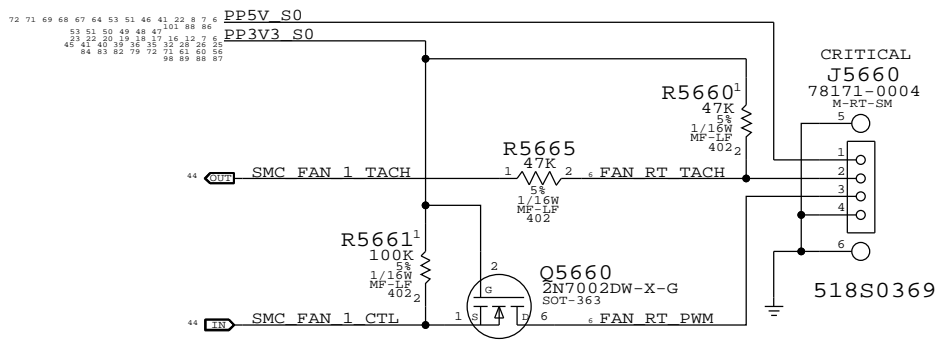
B

A

Left Fan



Right Fan



D

C

B

A

SYNC MASTER=K18_MLB		SYNC DATE=04/27/2010	
PAGE TITLE		Fan Connectors	
		DRAWING NUMBER	SIZE
		REVISION	D
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		PAGE	56 OF 132
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PSOC USB CONTROLLER

- USB INTERFACES TO MLB
- SPI HOST TO Z2
- TRACKPAD PICK BUTTONS
- KEYBOARD SCANNER

IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA	2.55 KOHM	0.0255 V	0.255E-6 W
	80UA			0.204 V	16.32E-6 W
3V3 LDO	VDD	60MA (MAX)	10 OHM	0.6 V	36E-3 W
	VOUT	60MA (MAX)	0.2 OHM	0.012 V	0.72E-3 W
PSOC	VDD	8MA (TYP)	1.5 OHM	0.012 V	96E-6 W
	14MA (MAX)			0.021 V	294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

Keyboard Connector

SMC Manual Reset & Isolation

Left shift, option & control keys combined with power button cause SMC RESET# assertion.
Keys ANDed with PSOC power to isolate when PSOC is not powered.

TPAD Buttons Disable

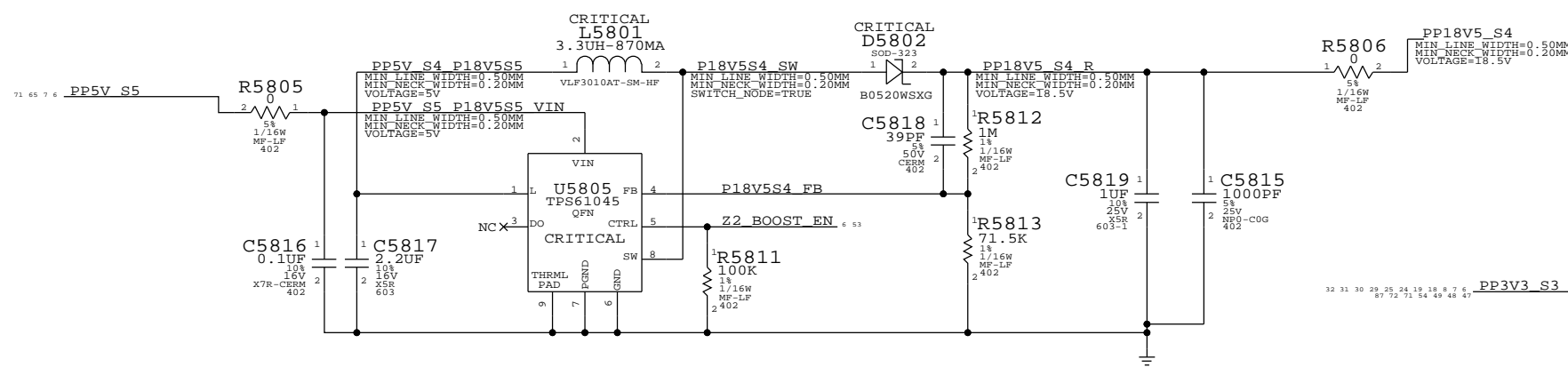
PLACE THESE COMPONENTS CLOSE TO J5800
THIS ASSUMES THERE'S A PP3V42_G3H PULL UP ON MLB

THE TPAD BUTTONS WILL BE DISABLE
WHEN THE LID IS CLOSED
LID OPEN => SMC_LID_LC ~ 3.42V
LID CLOSE => SMC_LID_LC < 0.50V

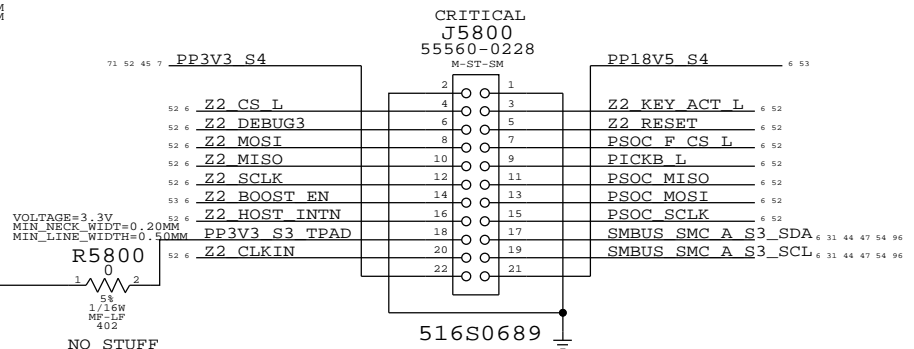
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WELLSPRING 1		DRAWING NUMBER	SIZE D
Apple Inc.		REVISION	
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BOOSTER +18.5VDC FOR SENSORS

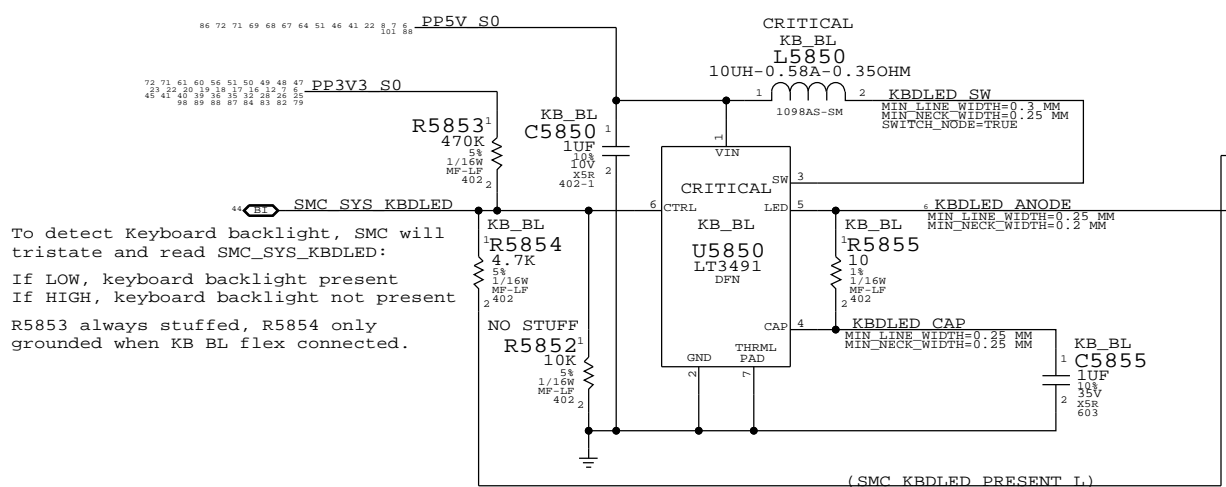
- BOOSTER DESIGN CONSIDERATION:
- POWER CONSUMPTION
 - DROOP LINE REGULATION
 - RIPPLE TO MEET ERS
 - 100-300 KHZ CLEAN SPECTRUM
 - STARTUP TIME LESS THAN 2MS
 - R5812,R5813,C5818 MODIFIED



IPD Flex Connector

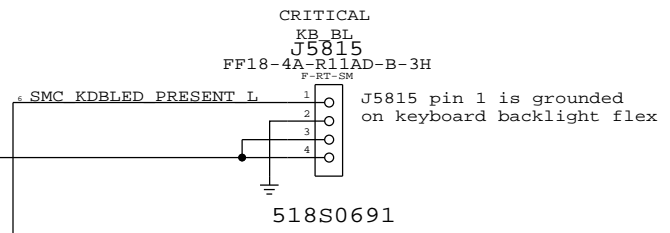


Keyboard Backlight Driver & Detection




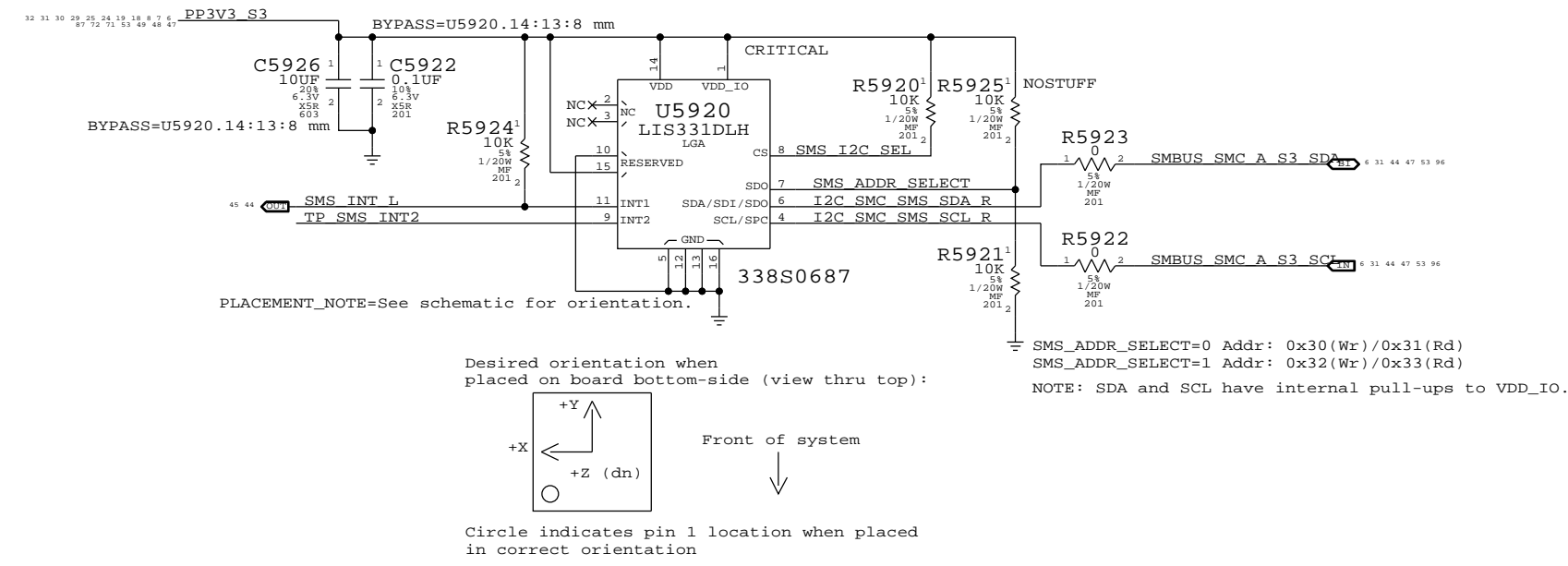
To detect Keyboard backlight, SMC will tristate and read SMC_SYS_KBDLED:
If LOW, keyboard backlight present
If HIGH, keyboard backlight not present
R5853 always stuffed, R5854 only grounded when KB BL flex connected.

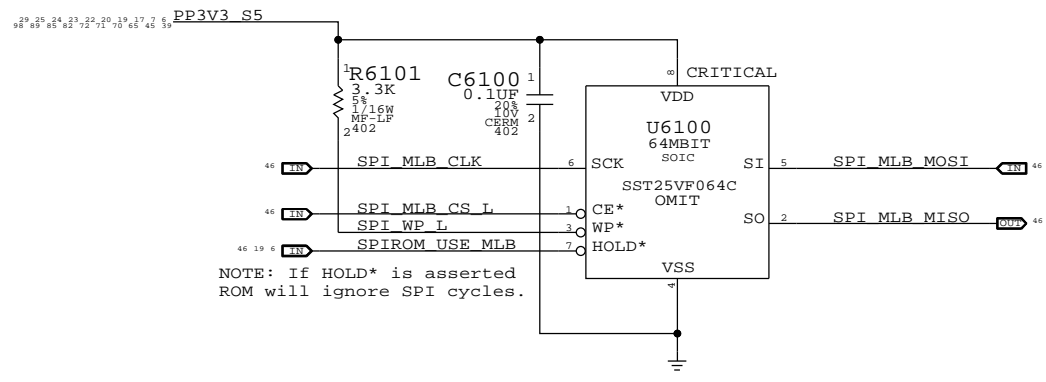
Keyboard Backlight Connector

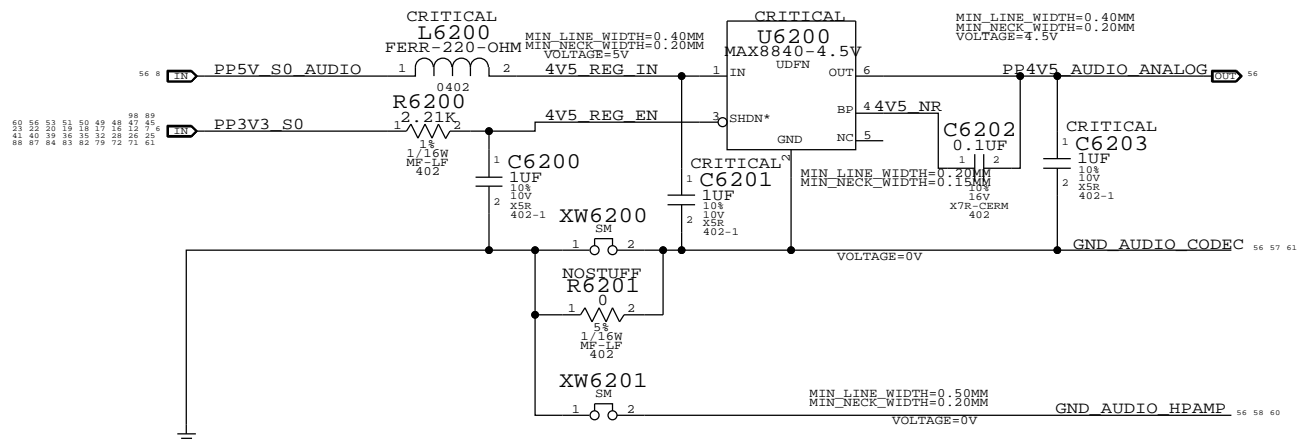


J5815 pin 1 is grounded on keyboard backlight flex


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PAGE TITLE			
WELLSPRING 2			
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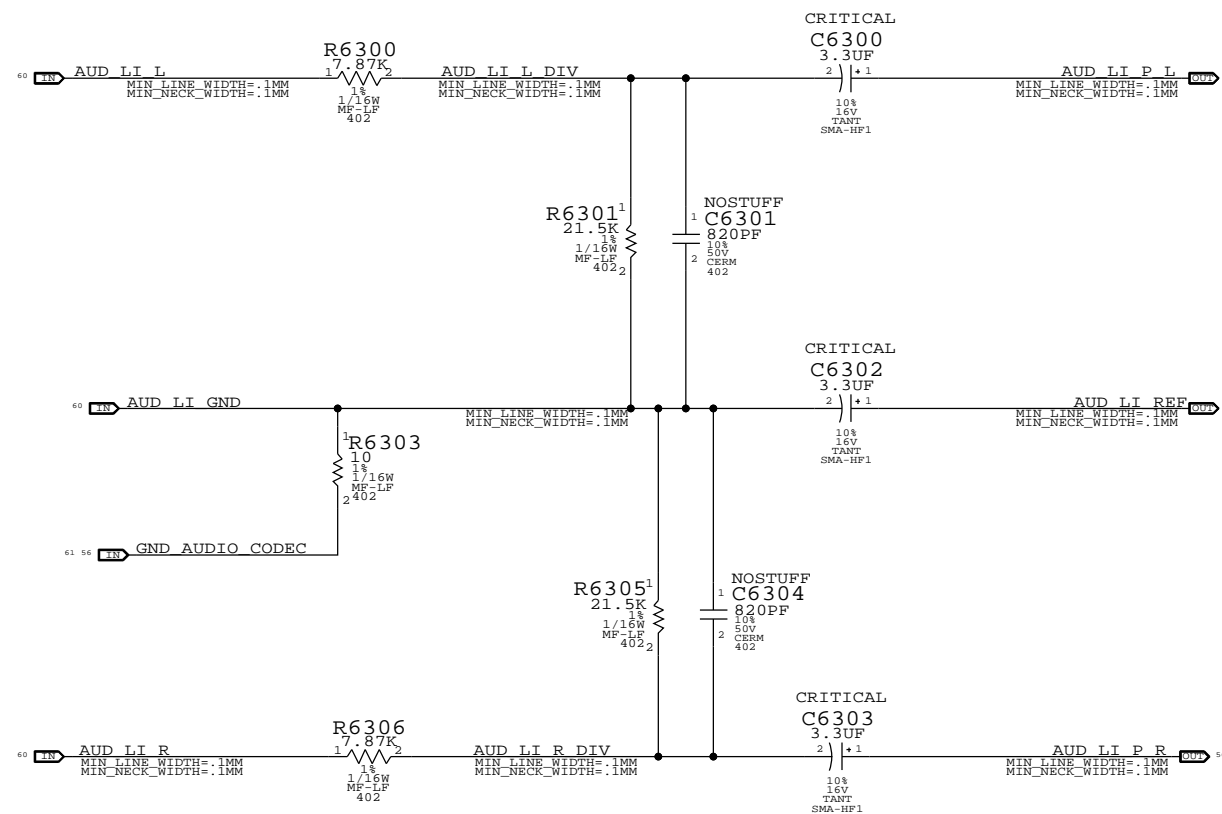


```
DIFF FSINPUT= 2.45VRMS
SE FSINPUT= 1.22VRMS
DAC1 FSOUTPUT= 1.34VRMS
DAC2/3 FSOUTPUTDIFF= 2.67VRMS
DAC2/3 FSOUTPUTSE= 1.34VRMS
```

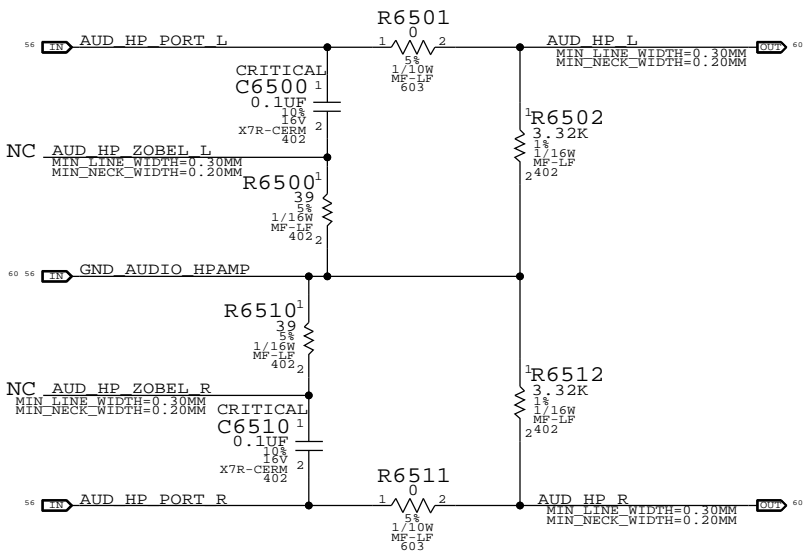
SYNC MASTER=K91 AUDIO		SYNC DATE=09/30/2010	
PAGE TYPE			
AUDIO: CODEC/REGULATOR			
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LINE INPUT VOLTAGE DIVIDER

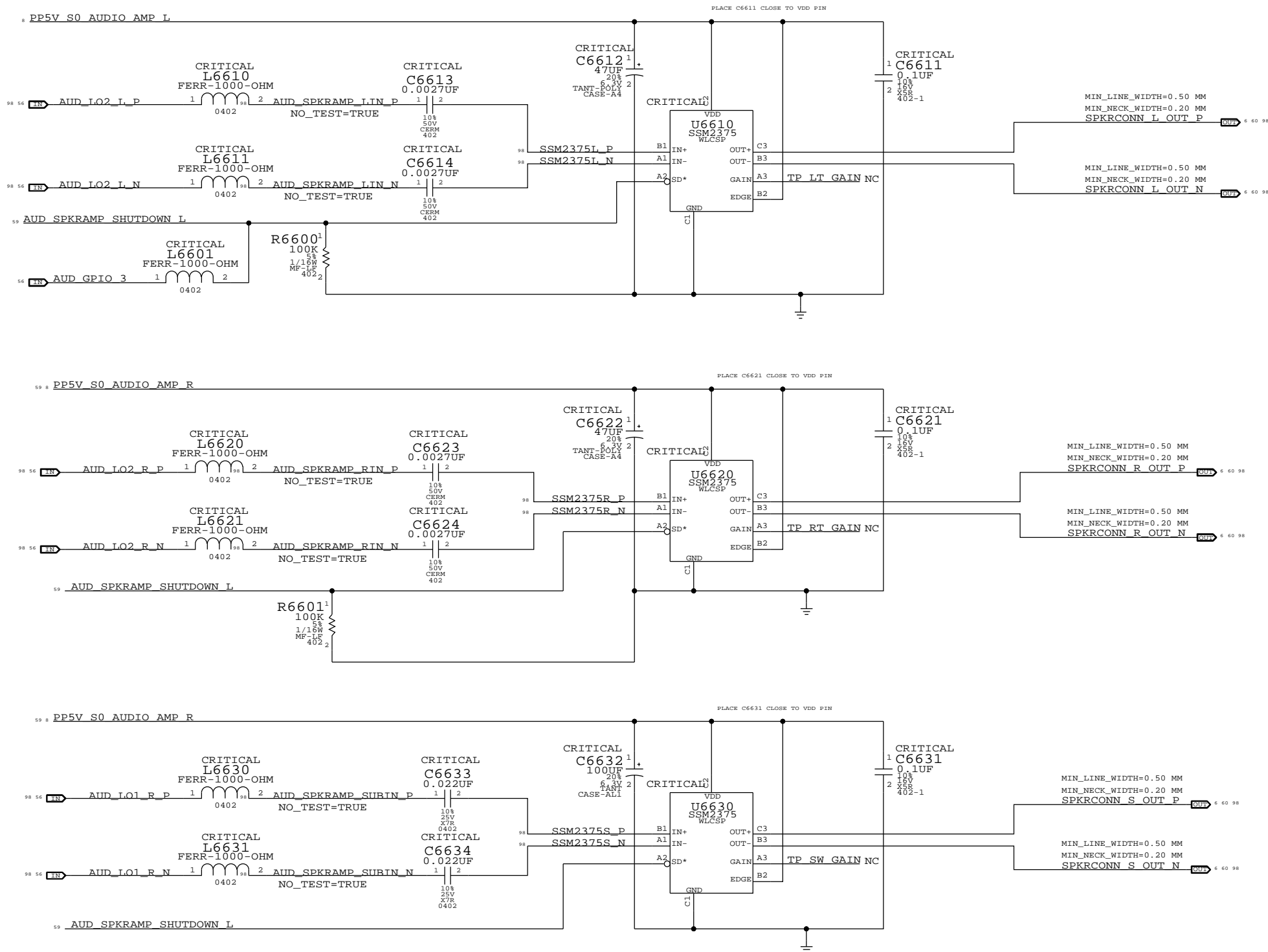
CODEC RIN = 20K OHMS
NET RIN = 18K OHMS
FC = 8 HZ
VIN = 2VRMS, CODEC VIN = 1.14 VRMS




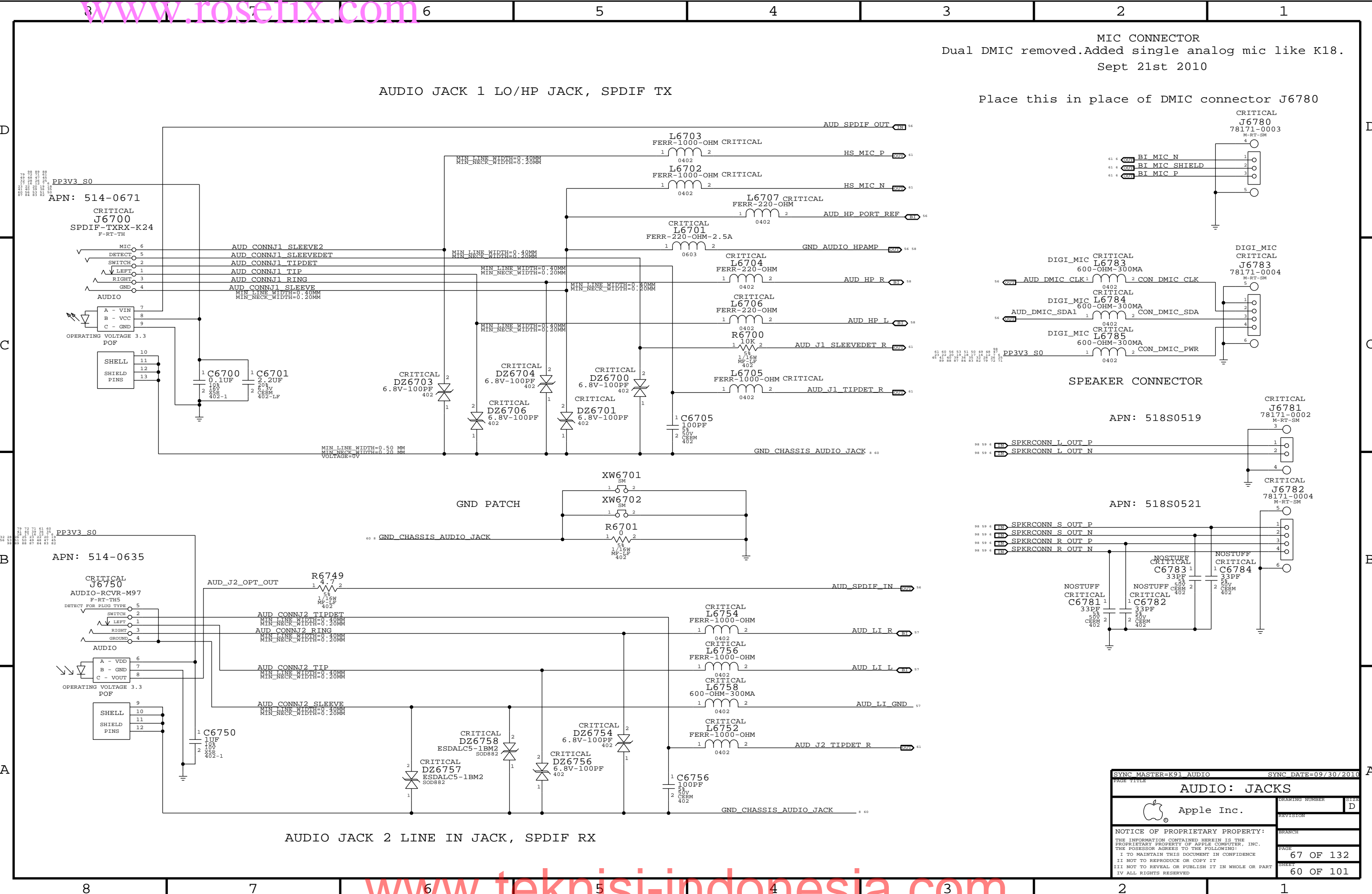
ZOBEL NETWORK & 1ST ORDER DAC FILTER PLACEHOLDER



3X MONO SPEAKER AMPLIFIERS (SSM2375)
APN: 353S2958
GAIN = +3 DB
1ST ORDER FC (L&R) = ~737 HZ
1ST ORDER FC (SUB) = ~90 HZ



SYNC MASTER=K91 AUDIO		SYNC DATE=07/12/2010	
PAGE TITLE			
AUDIO: SPEAKER AMP			
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	PAGE		
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PAGE TITLE		AUDIO: JACKS	
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CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP/LINE OUT	0X02 (2)	0X02 (2)	0X09 (9,A)	N/A	0X09 (A)
SATELLITES	0X04 (4)	0X04 (4)	0X0B (11)	GPIO_3	N/A
SUB	0X03 (3)	0X03 (03)	0X0A (10)	GPIO_3	N/A
SPDIF OUT	N/A	0X08 (8)	0X10 (16)	N/A	0X0C (B)

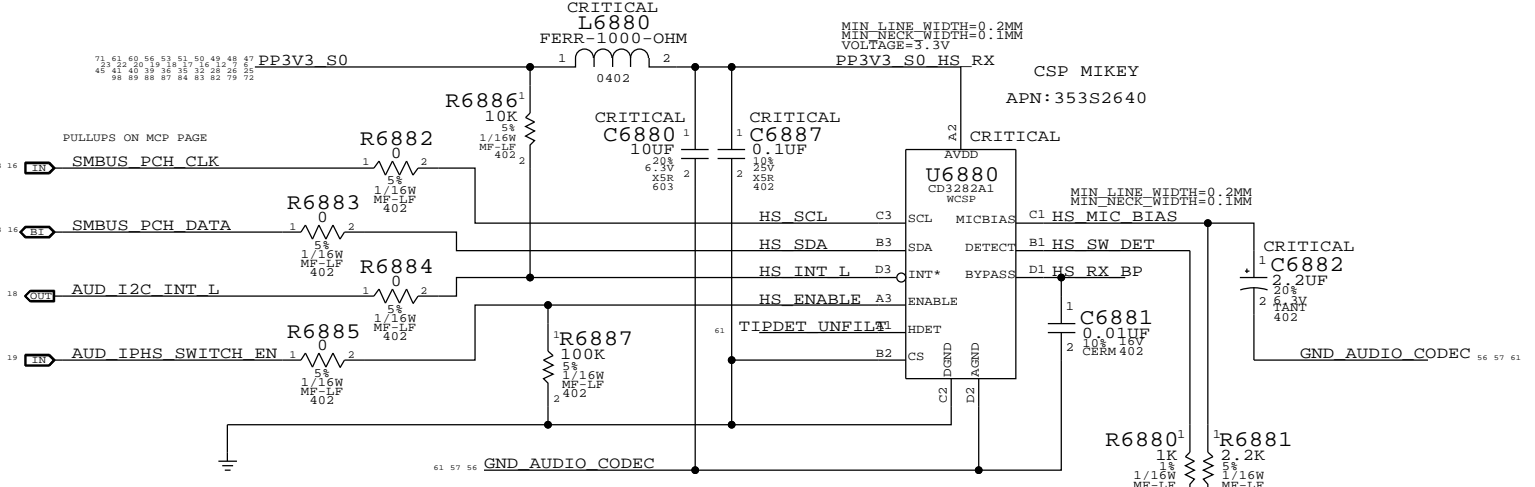
CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
LINE IN	0X05 (5)	0X0C (12,C)	N/A	0X0C (12,C)
SPDIF IN	0X07 (7)	0X0F (15)	N/A	N/A
BUILT-IN MIC	0X06 (6)	0X0D (13)	N/A	N/A
HEADSET MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	MIKEY	MIKEY

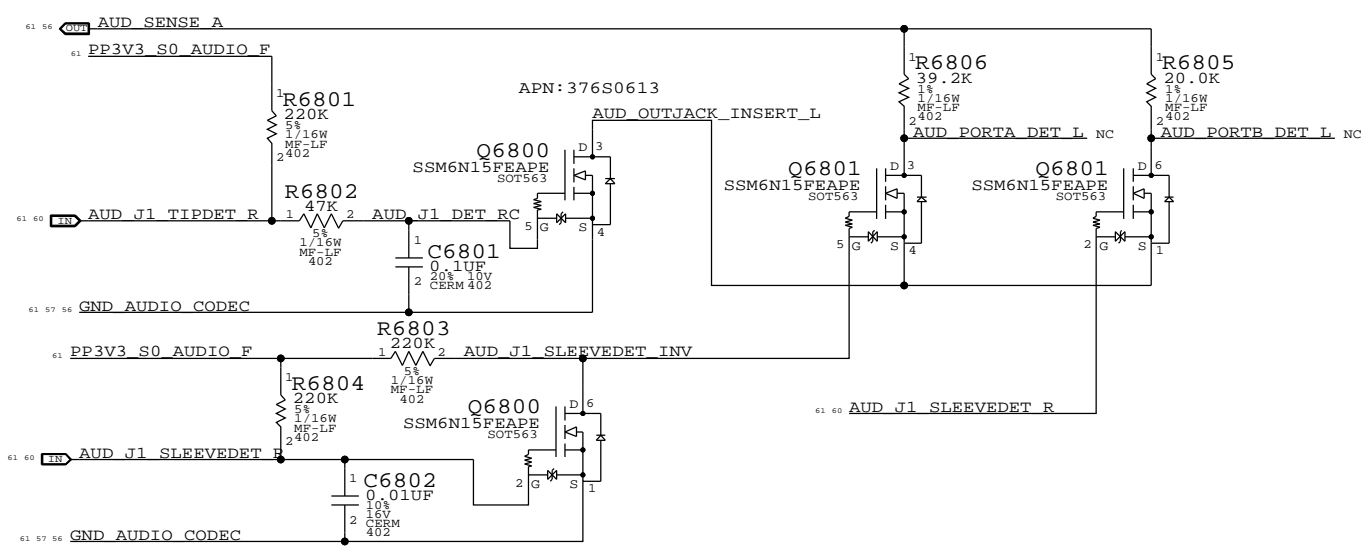
SYSTEM INT AND GPIO LINES

FUNCTION	INT	GPIO
MIKEY ENABLE		SATA4GP/GPIO 16
MIKEY INTERRUPT	PIRQ H	GPIO 5
PERIPHERAL DETECT	PIRQ F	GPIO 3

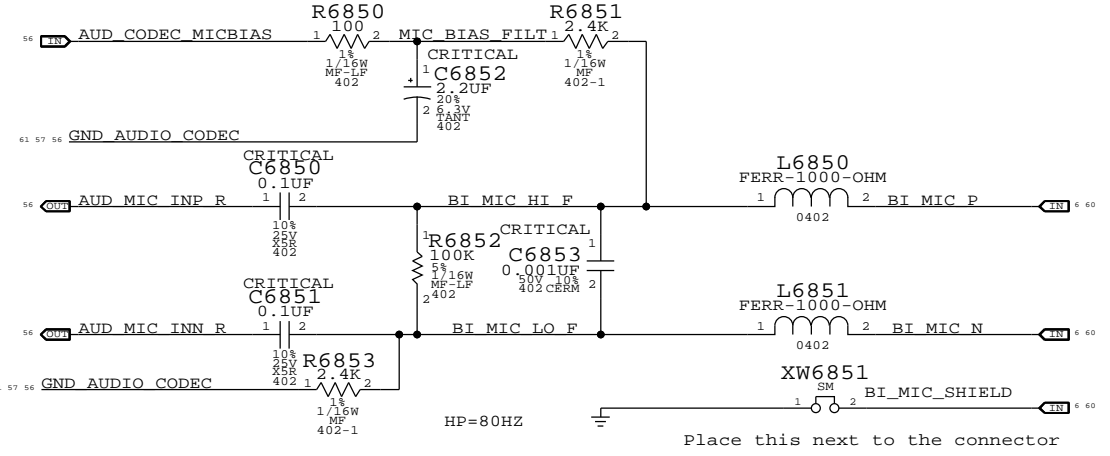
PORT B LEFT(HEADSET MIC)
HP=80HZ, LP=8.82KHZ



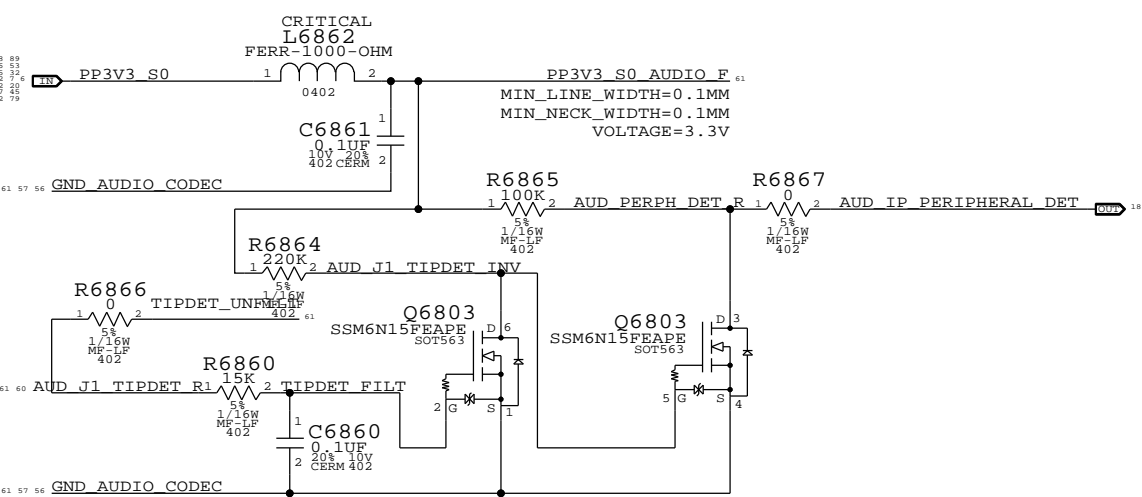
PORT A DETECT (HEADPHONES) PORT B DETECT (SPDIF DELEGATE)



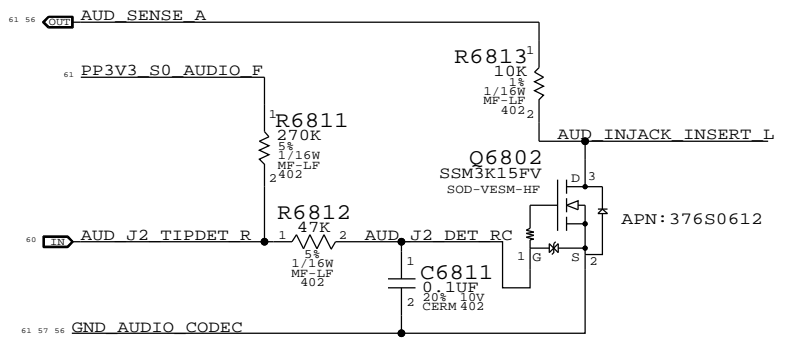
PORT B RIGHT (BUILT-IN MIC)



EXTRACTION NOTIFICATION

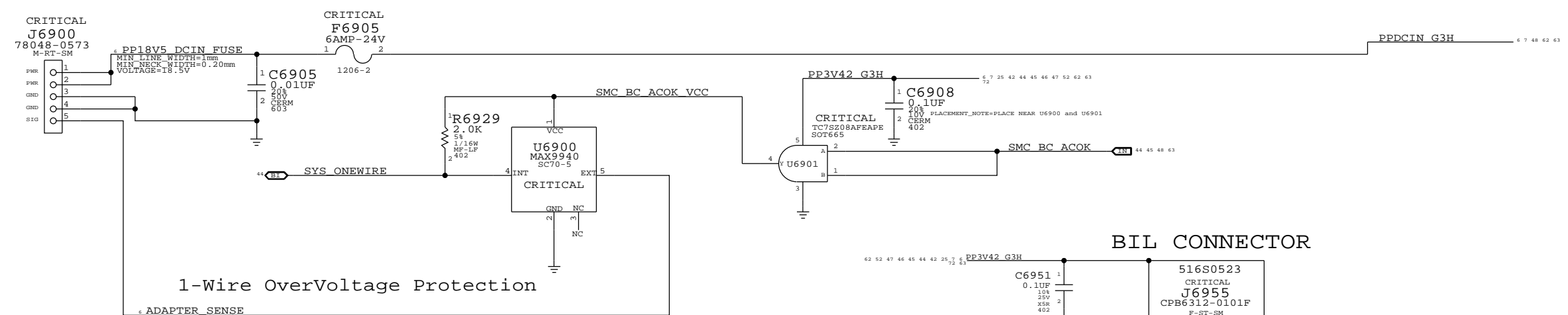


PORT C DETECT (LINE-IN)

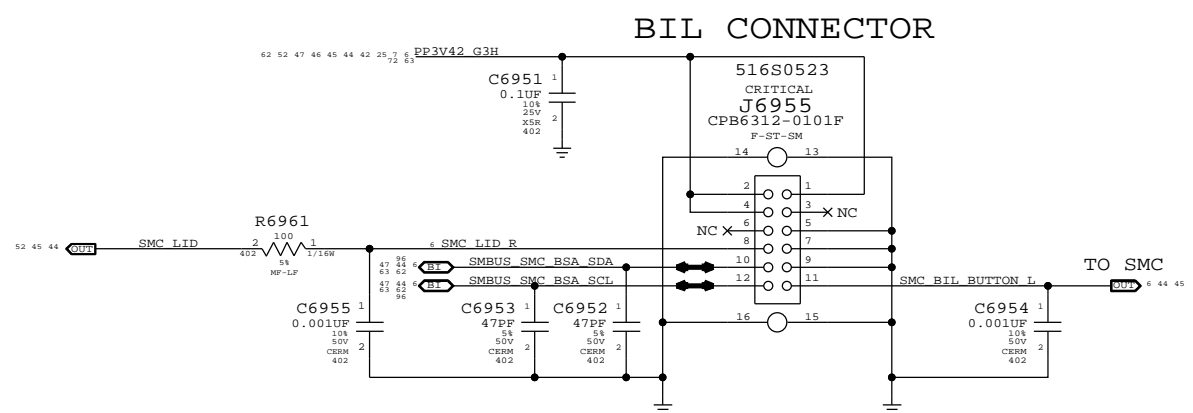


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PAGE TITLE			
AUDIO: JACK TRANSLATORS			
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MagSafe DC Power Jack

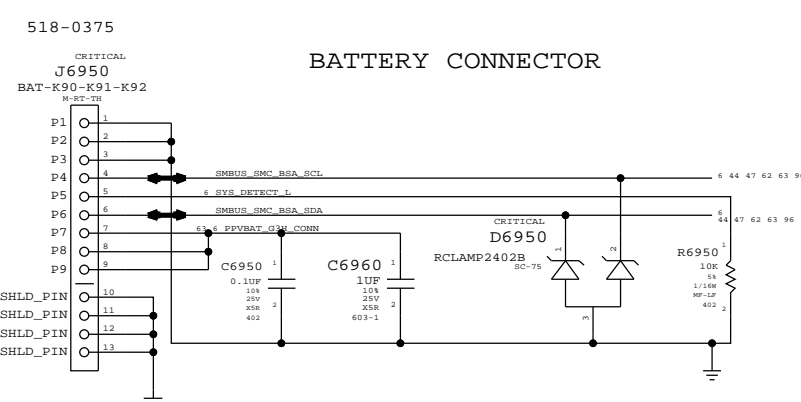
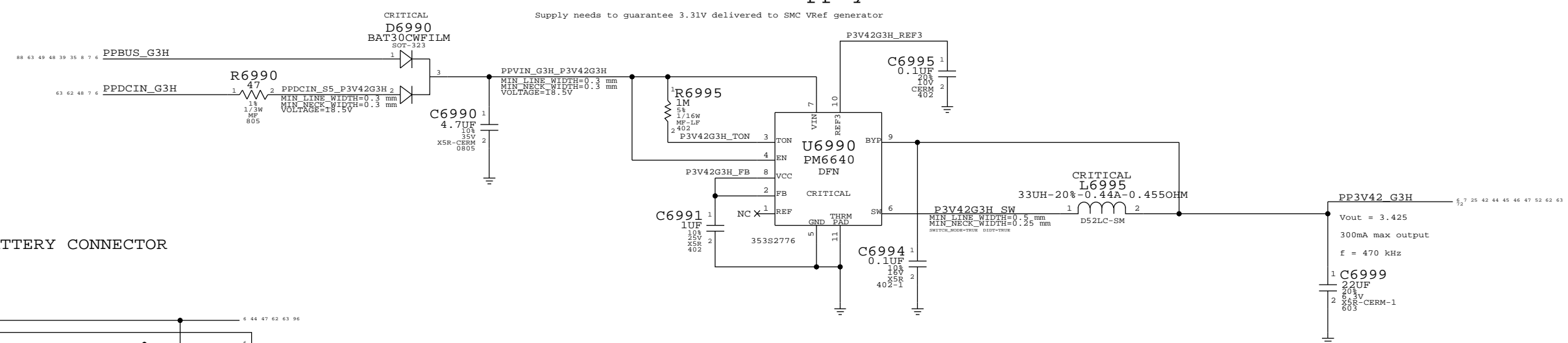



The chassis ground will otherwise float and can send transients onto ADAPTER_SENSE when AC is connected.

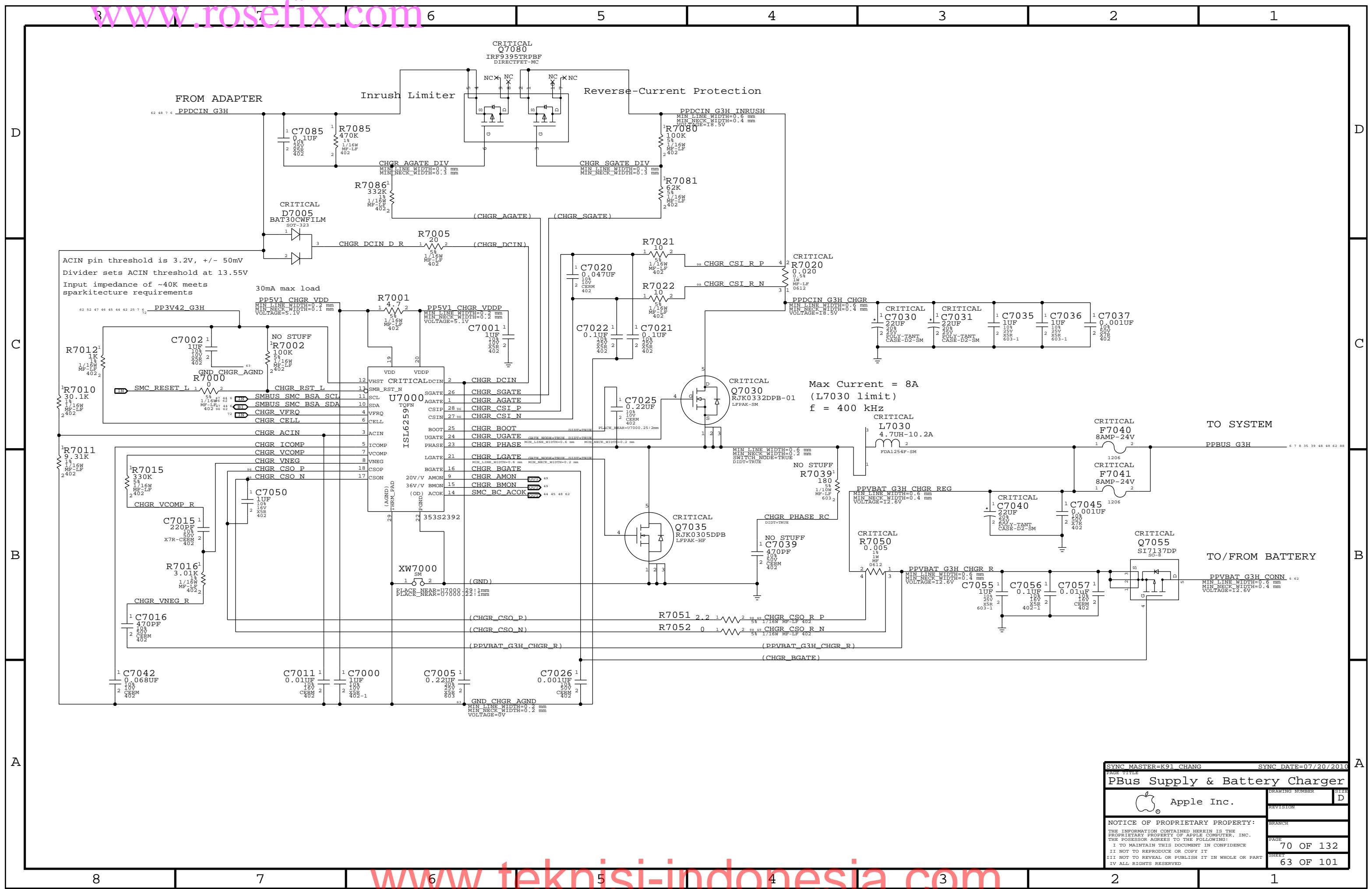



3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator




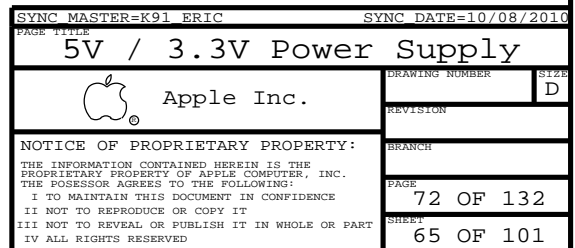
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PAGE TITLE			
DC-In & Battery Connectors			
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		REVISION	D
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SYNC MASTER=K91 CHANG		SYNC DATE=07/20/2010	
PAGE TITLE			
PBus Supply & Battery Charger			
 Apple Inc.		DRAWING NUMBER	SIZE
		REVISION	D
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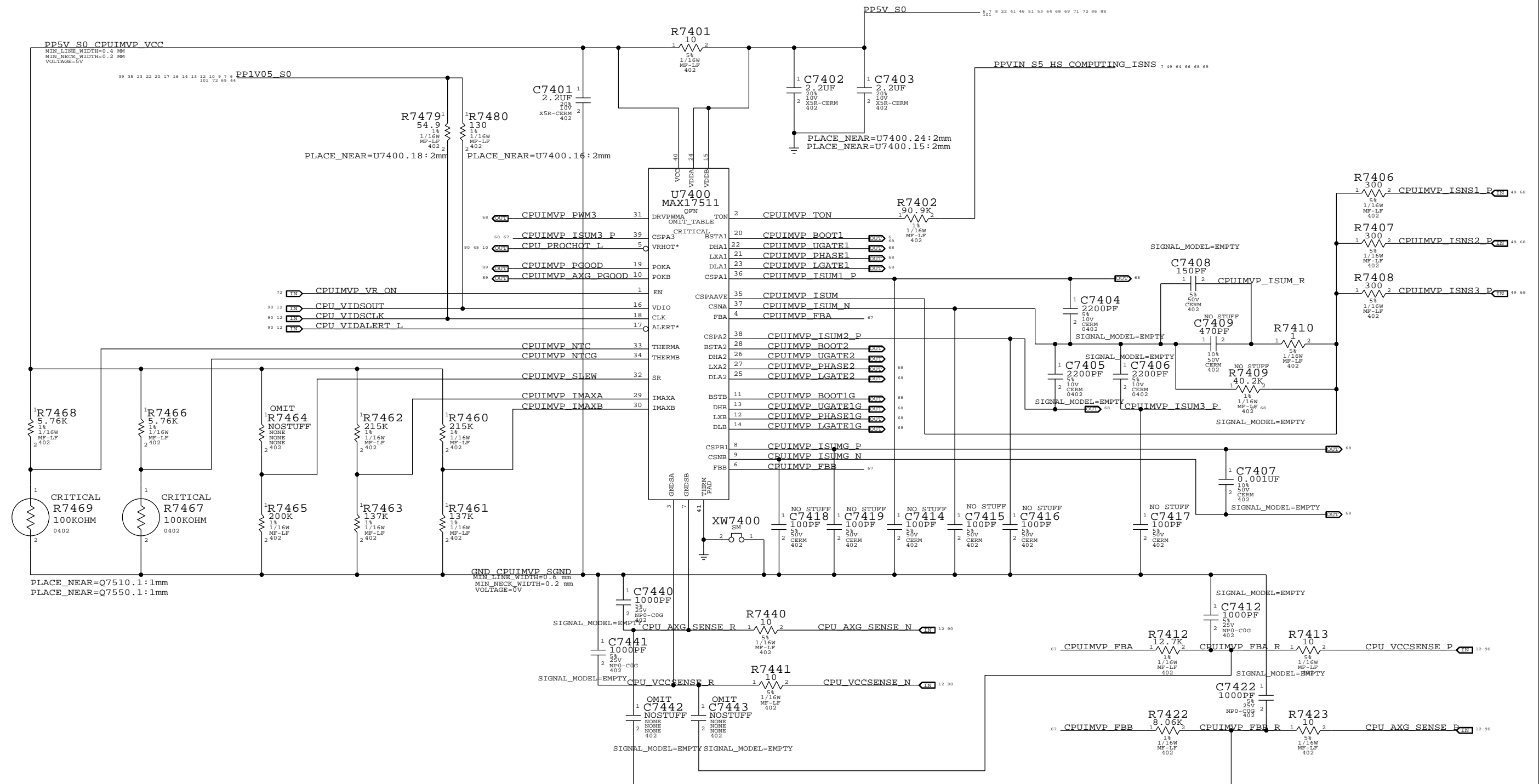

$$\begin{aligned} \text{OCP} &= R_{7141} \times 8.5\mu\text{A} / R_{7140} \\ \text{OCP} &= 8.5\text{A} \end{aligned}$$

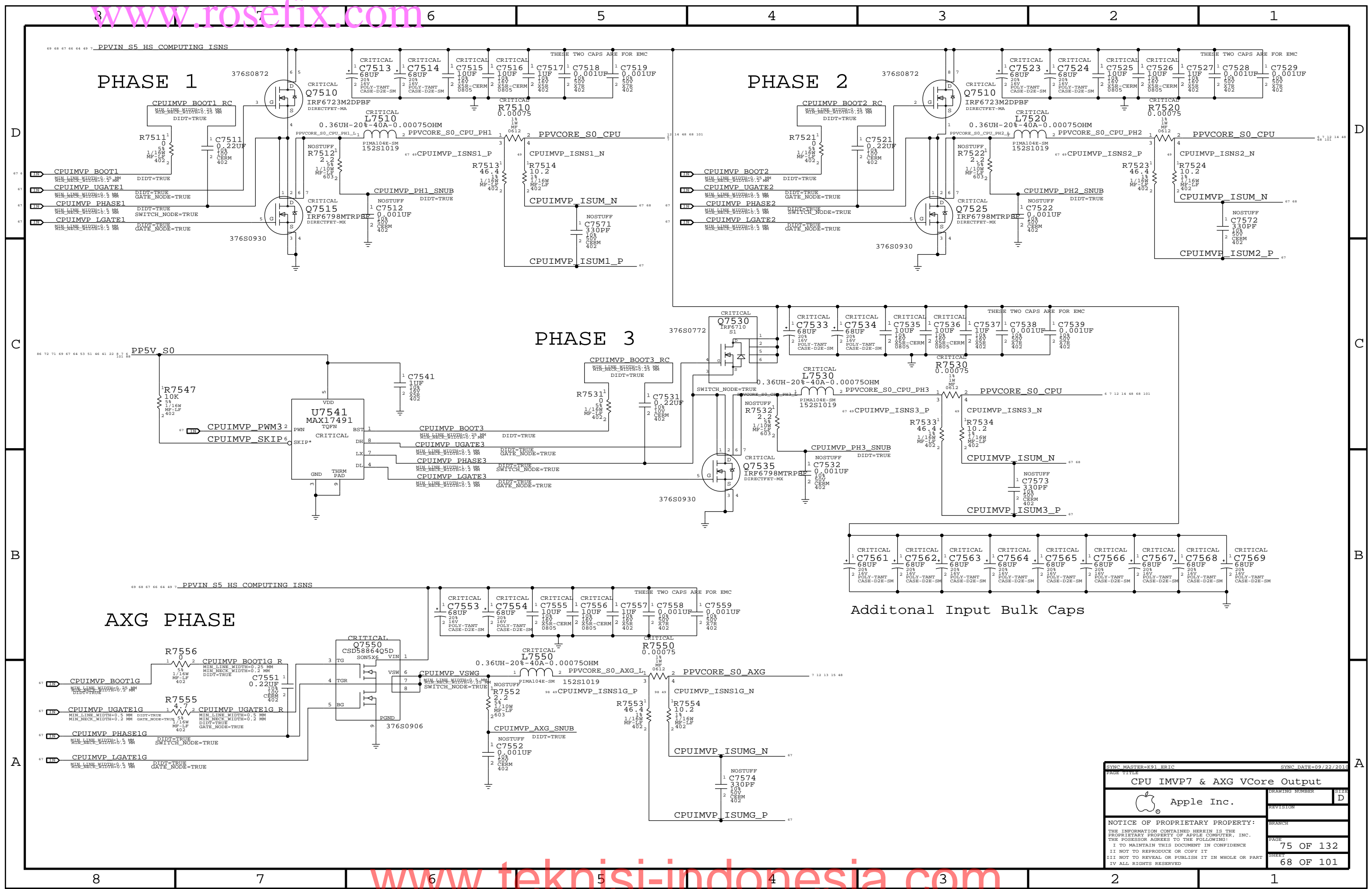
SYNC MASTER-K91 ERIC		SYNC DATE=10/08/2010	
PAGE TITLE			
System Agent Supply			
	Apple Inc.	DRAWING NUMBER	SIZE
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		SHEET 64 OF 101	




1

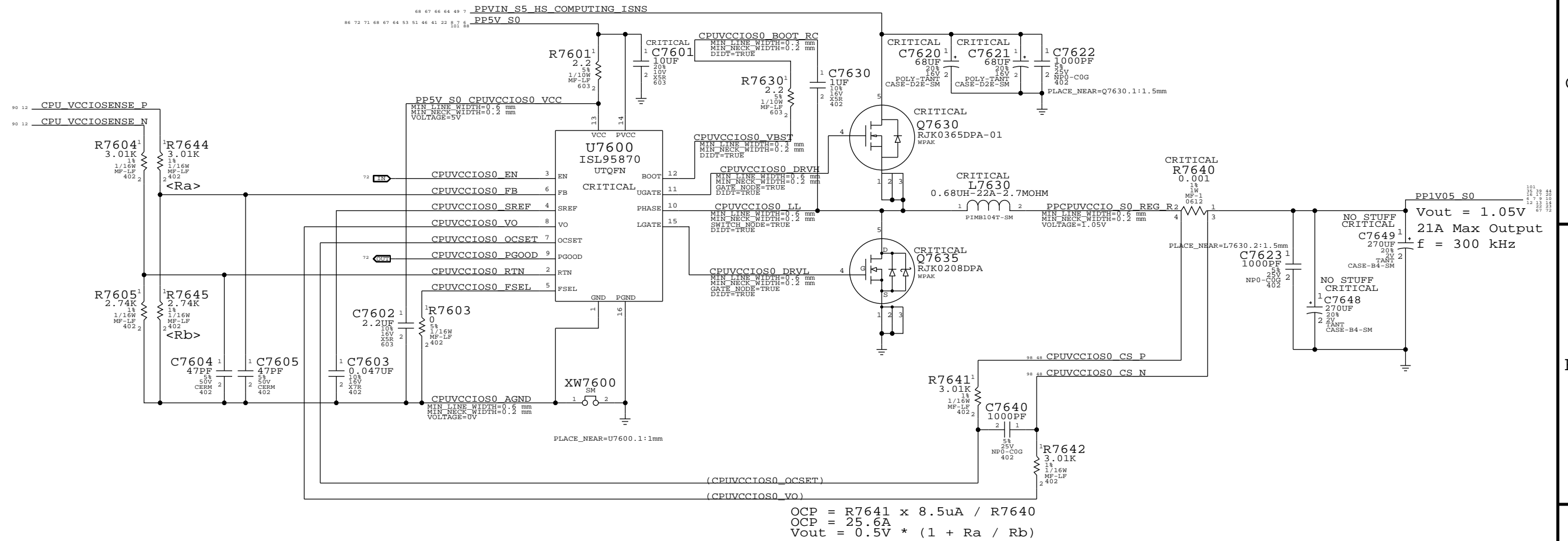
SYNC MASTER=K91.ERIC		SYNC DATE=10/08/2016	
PAGE TITLE			
CPU IMVP7 & AXG VCore Regulator			
 Apple Inc.		DRAWING NUMBER	SIZE D
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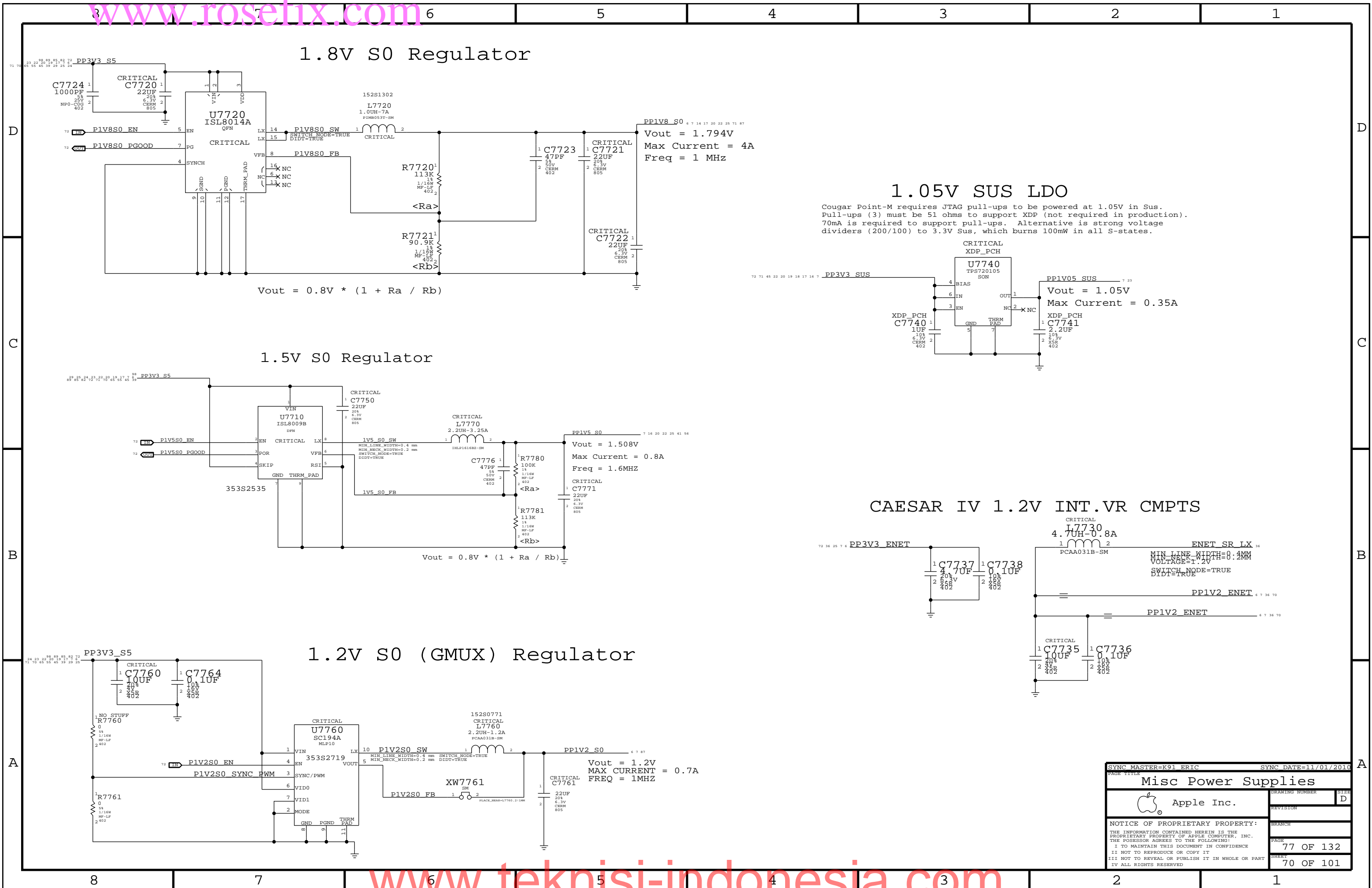


SYNC MASTER=K91 ERIC		SYNC DATE=09/22/2010	
PAGE TITLE			
CPU IMVP7 & AXG VCore Output			
 Apple Inc.		DRAWING NUMBER	SIZE
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		REVISION	
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CPU VCCIO (1.05V S0) Regulator



SYNC MASTER=K91 ERIC		SYNC DATE=10/08/2010	
PAGE TITLE			
CPU VCCIO (1.05V) Power Supply			
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1.8V S0 Regulator

Vout = 1.794V
Max Current = 4A
Freq = 1 MHz

1.05V SUS LDO

Cougar Point-M requires JTAG pull-ups to be powered at 1.05V in Sus. Pull-ups (3) must be 51 ohms to support XDP (not required in production). 70mA is required to support pull-ups. Alternative is strong voltage dividers (200/100) to 3.3V Sus, which burns 100mW in all S-states.

Vout = 1.05V
Max Current = 0.35A

1.5V S0 Regulator


Vout = 1.508V
Max Current = 0.8A
Freq = 1.6MHZ

CAESAR IV 1.2V INT.VR CMPTS

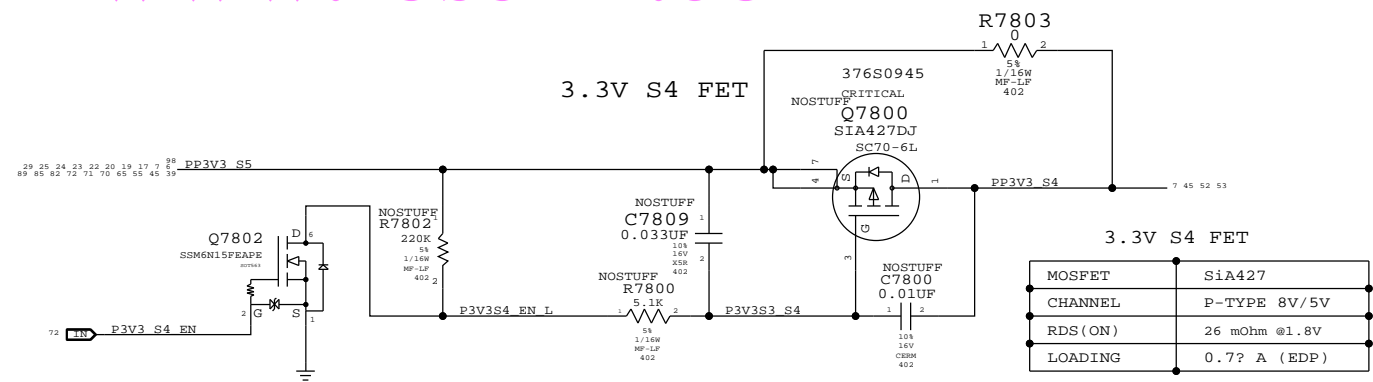
MIN LINE WIDTH=0.4MM
MIN SPACE=0.2MM
VOLTAGE=1.2V
SWITCH NODE=TRUE
BIDD=TRUE

1.2V S0 (GMUX) Regulator

Vout = 1.2V
MAX CURRENT = 0.7A
FREQ = 1MHZ

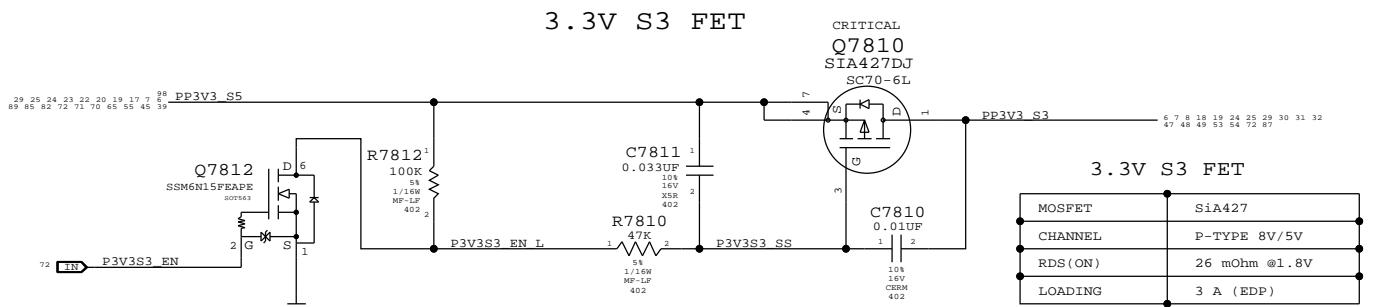
SYNC MASTER=K91 ERIC		SYNC DATE=11/01/2010	
PAGE TITLE			
Misc Power Supplies		DRAWING NUMBER	
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3.3V S4 FET



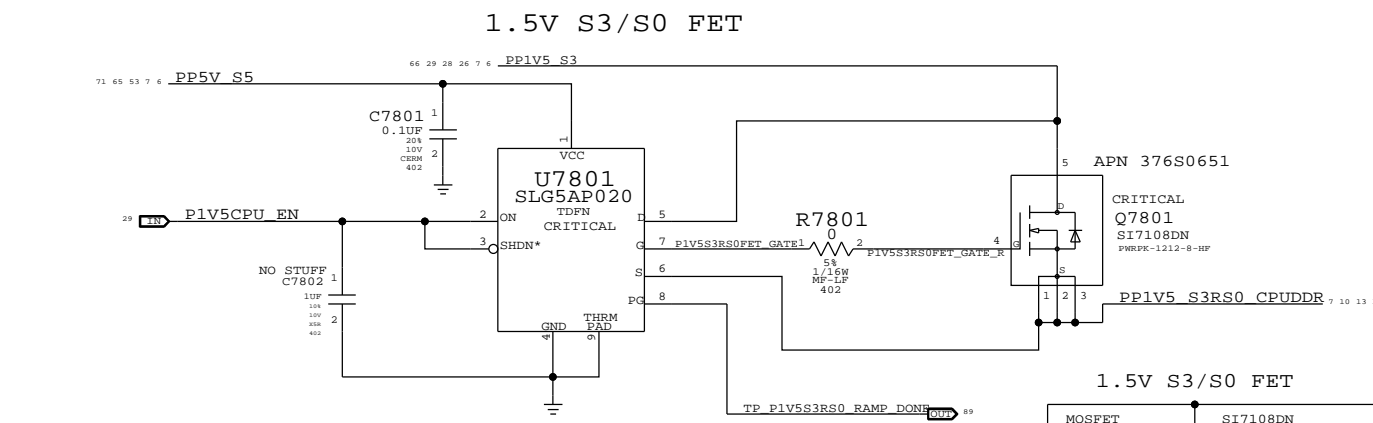
MOSFET	SIA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	0.7? A (EDP)

3.3V S3 FET



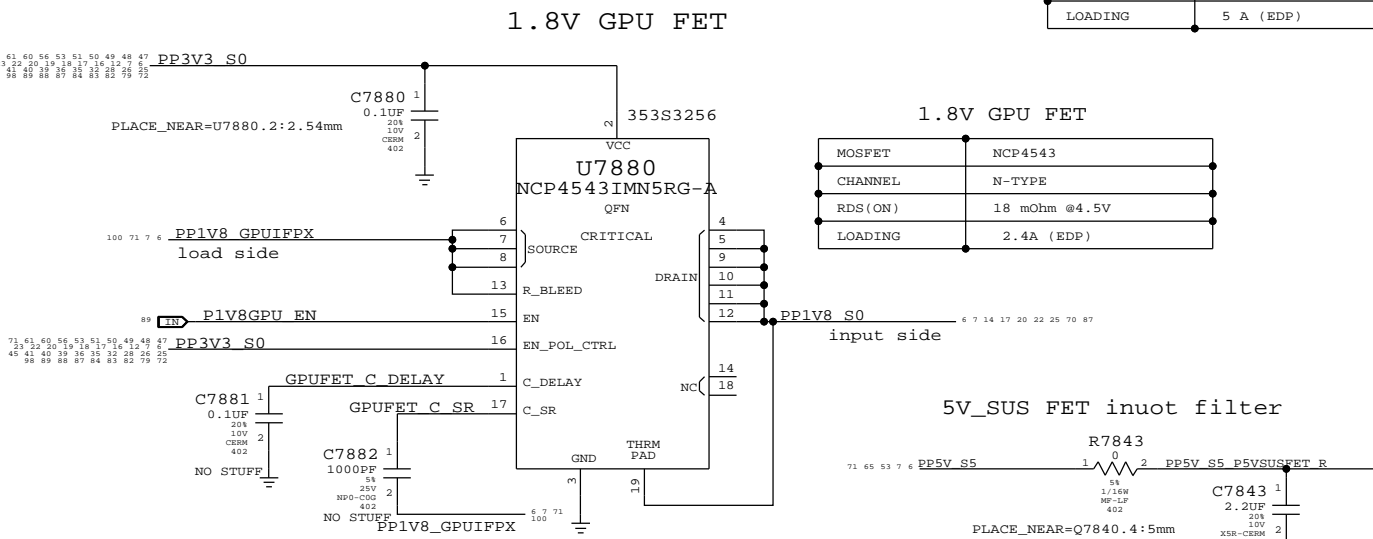
MOSFET	SIA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	3 A (EDP)

1.5V S3/S0 FET



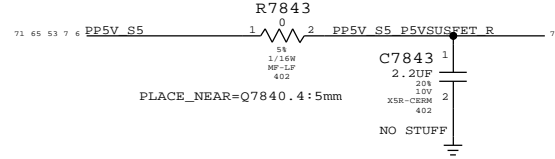
MOSFET	SI7108DN
CHANNEL	N-TYPE
RDS(ON)	6 mOhm @4.5V
LOADING	5 A (EDP)

1.8V GPU FET

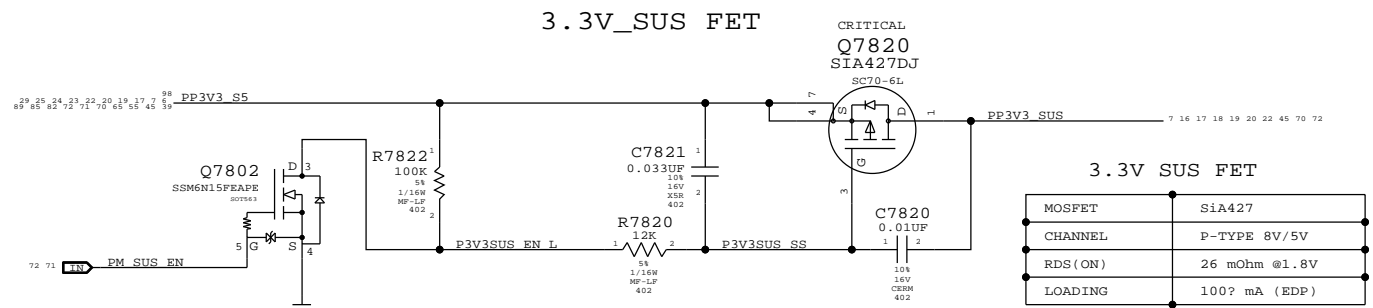


MOSFET	NCP4543
CHANNEL	N-TYPE
RDS(ON)	18 mOhm @4.5V
LOADING	2.4A (EDP)

5V_SUS FET inuot filter

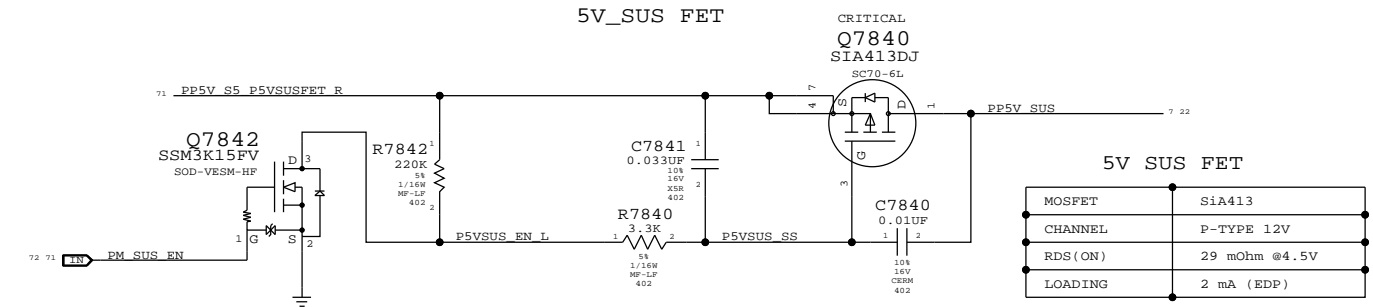


3.3V_SUS FET



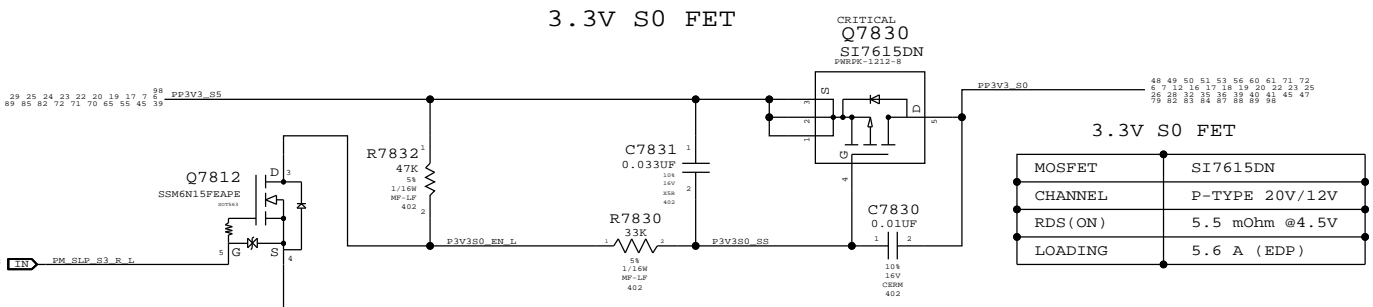
MOSFET	SIA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	100? mA (EDP)

5V_SUS FET



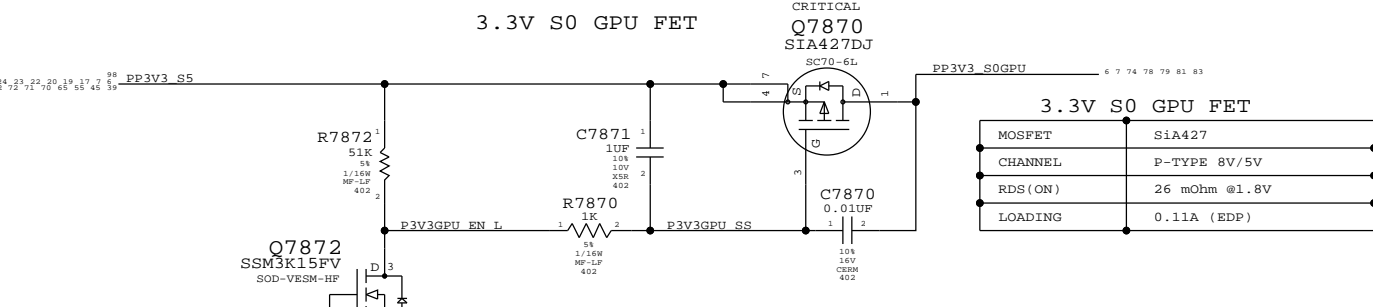
MOSFET	SIA413
CHANNEL	P-TYPE 12V
RDS(ON)	29 mOhm @4.5V
LOADING	2 mA (EDP)

3.3V S0 FET



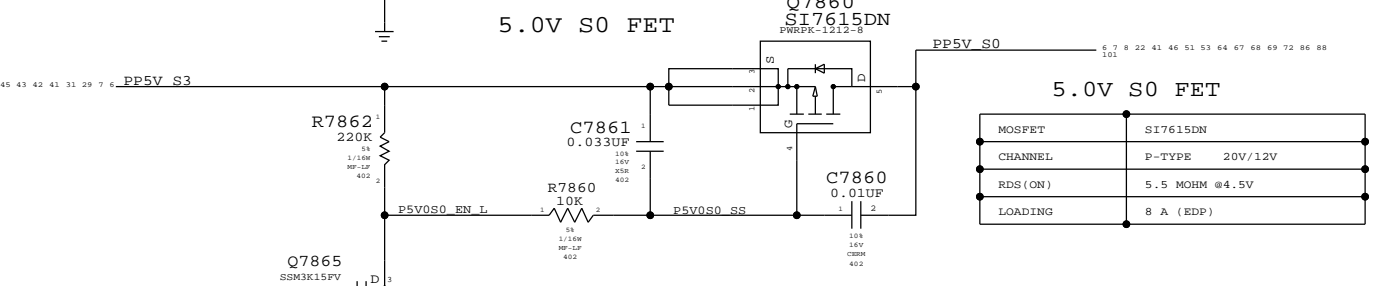
MOSFET	SI7615DN
CHANNEL	P-TYPE 20V/12V
RDS(ON)	5.5 mOhm @4.5V
LOADING	5.6 A (EDP)

3.3V S0 GPU FET



MOSFET	SIA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	0.11A (EDP)

5.0V S0 FET



MOSFET	SI7615DN
CHANNEL	P-TYPE 20V/12V
RDS(ON)	5.5 MOHM @4.5V
LOADING	8 A (EDP)

SYNC MASTER=K91 MARY

SYNC DATE=10/14/2010

Power FETs

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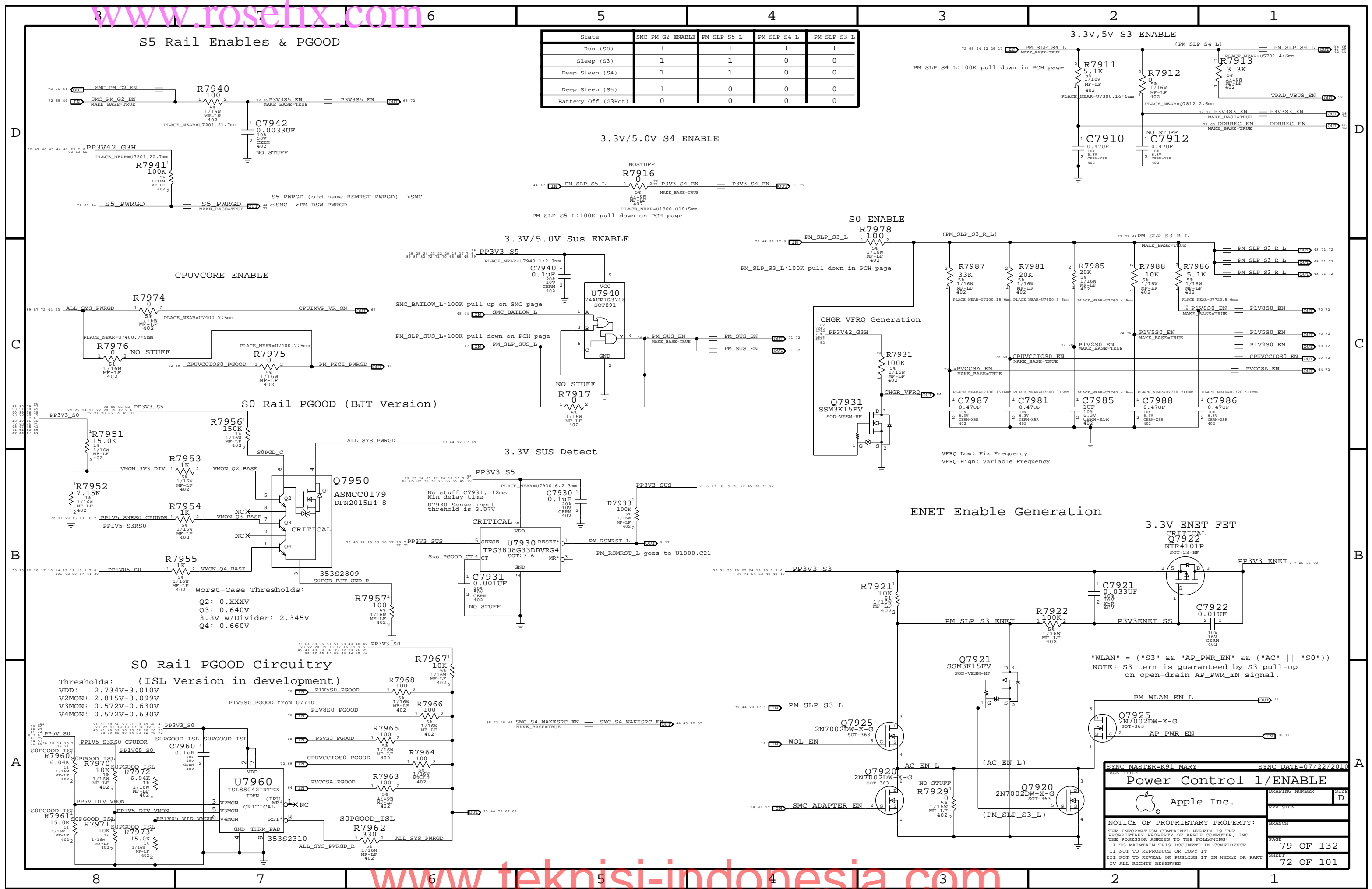
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Page Notes

Power aliases required by this page:

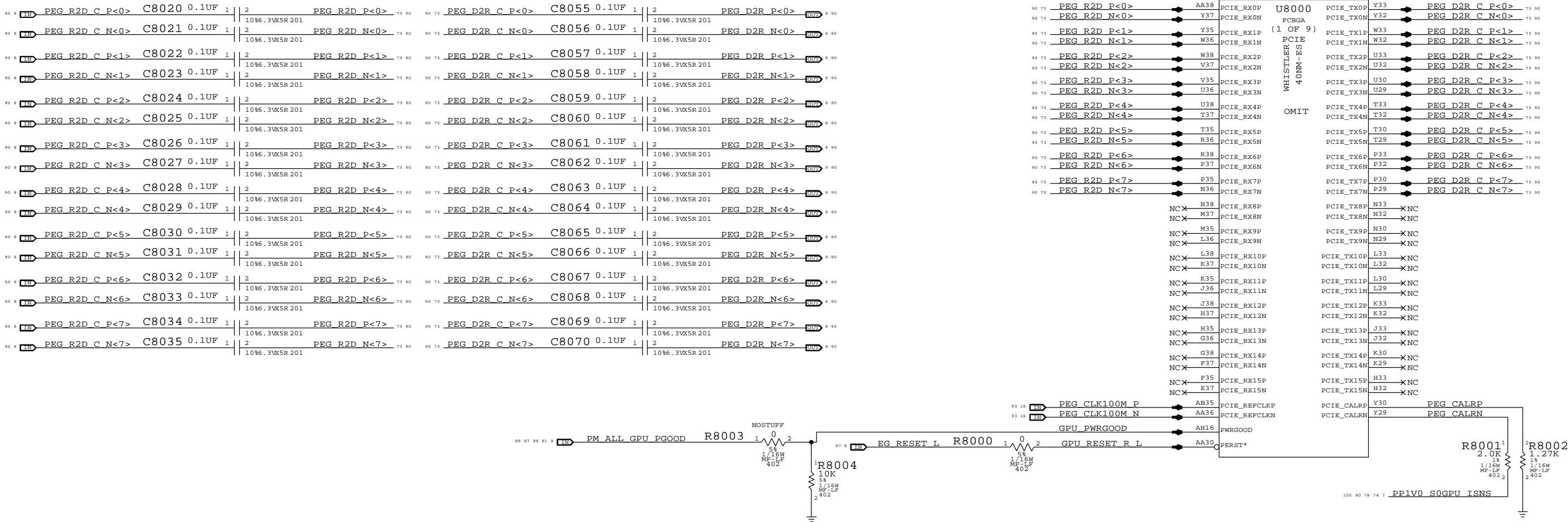
- =PP1V2_GPU_PEX_PLLEXVDD
- =PP1V2_GPU_PEX_IOVDDQ
- =PP1V2_GPU_PEX_IOVDD


Signal aliases required by this page:

(NONE)

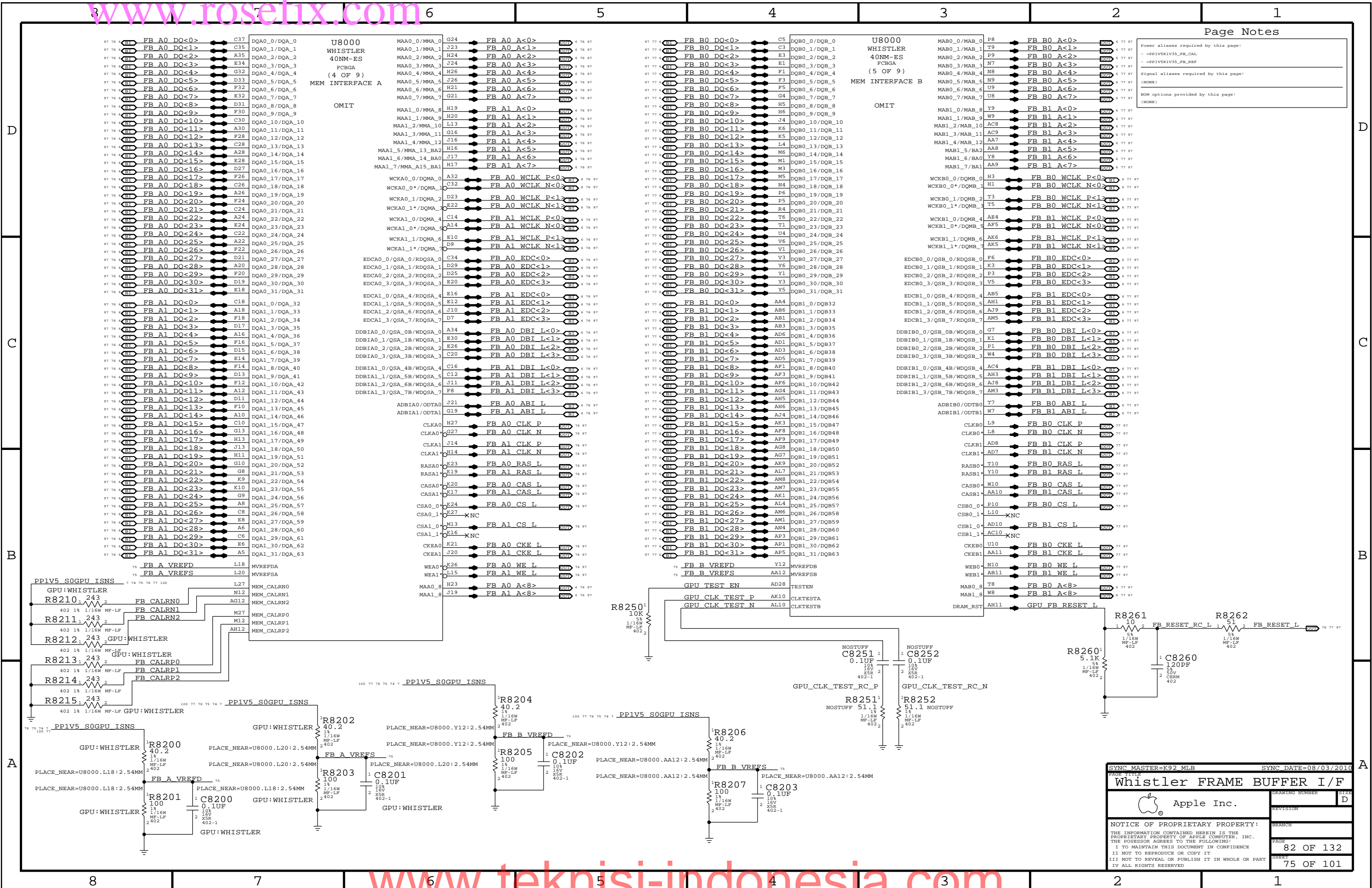
BOM options provided by this page:

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PAGE TITLE			
Whistler PCI-E		DRAWING NUMBER	SIZE
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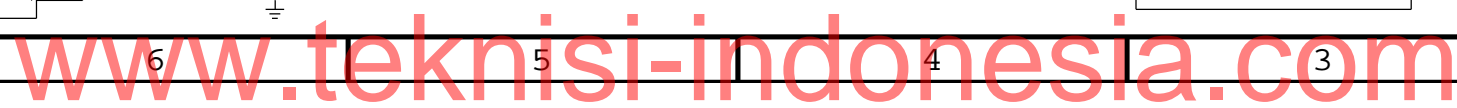




Power aliases required by this page:
- PPIV5SRIV35_FB_CAL
- PPIV5SRIV35_FB_REF

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



Page Notes

Power aliases required by this page:
- PP1V5_S0GPU_ISNS

Signal aliases required by this page:
(NONE)

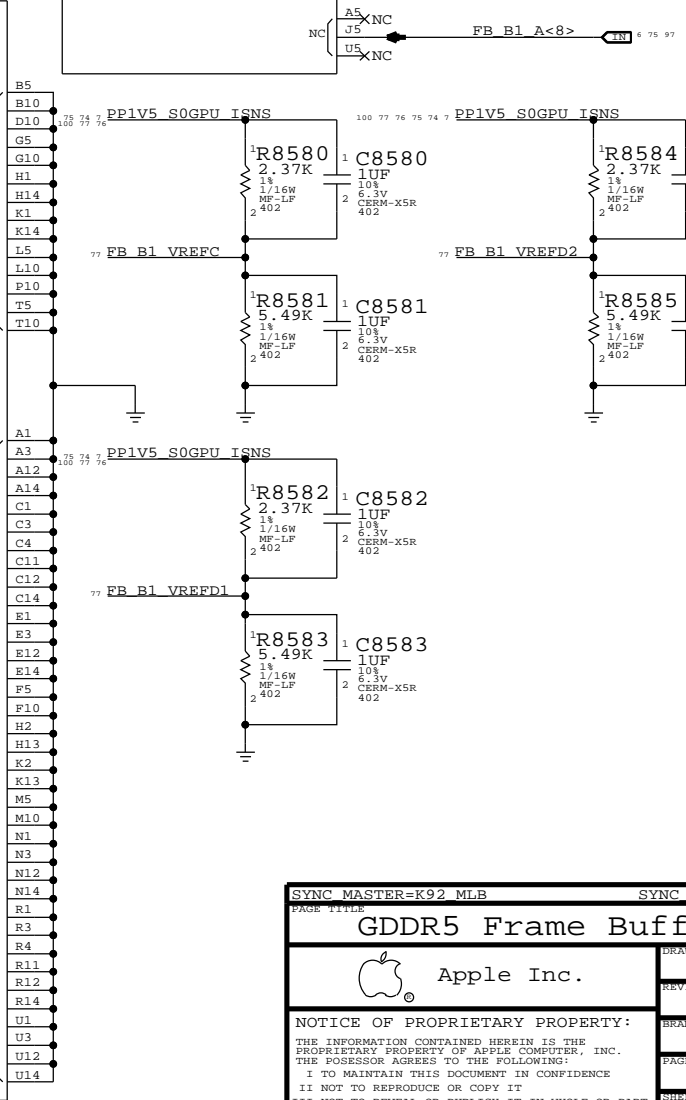
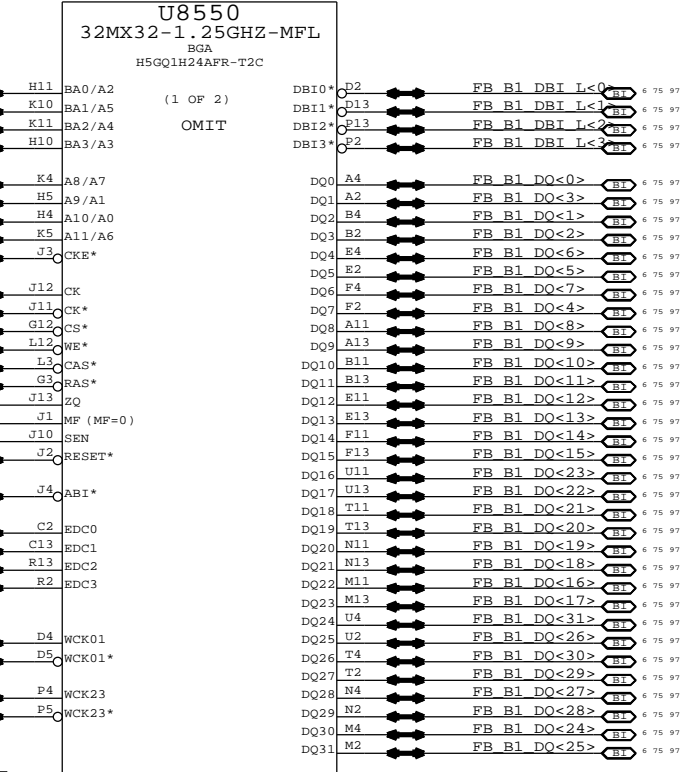
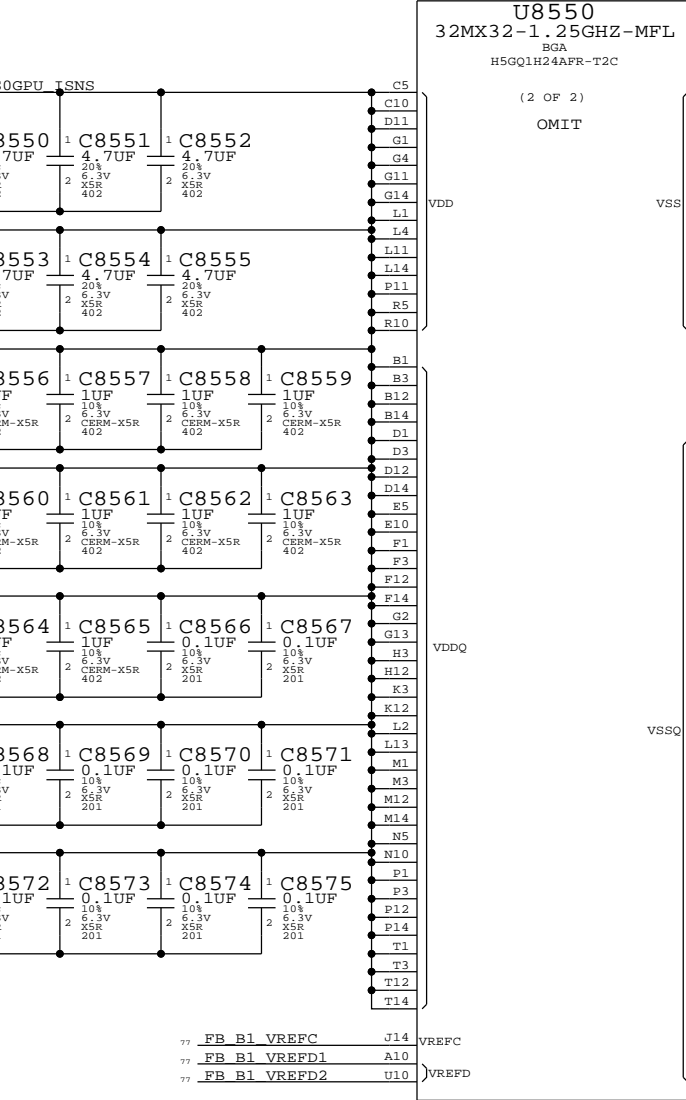
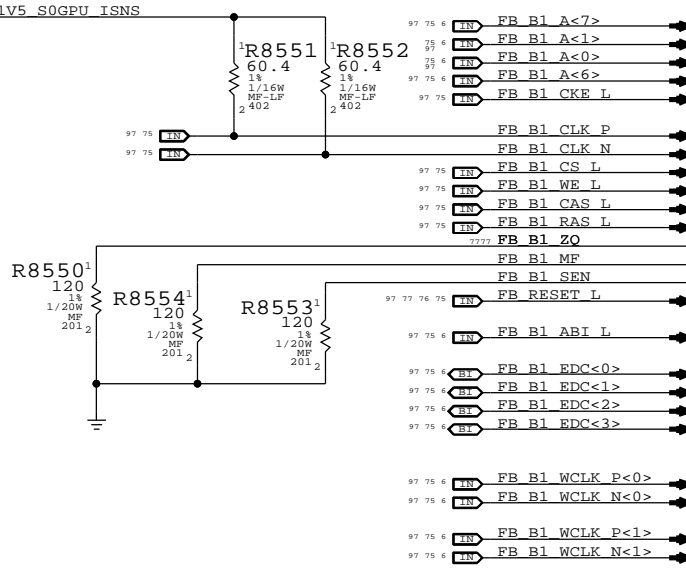
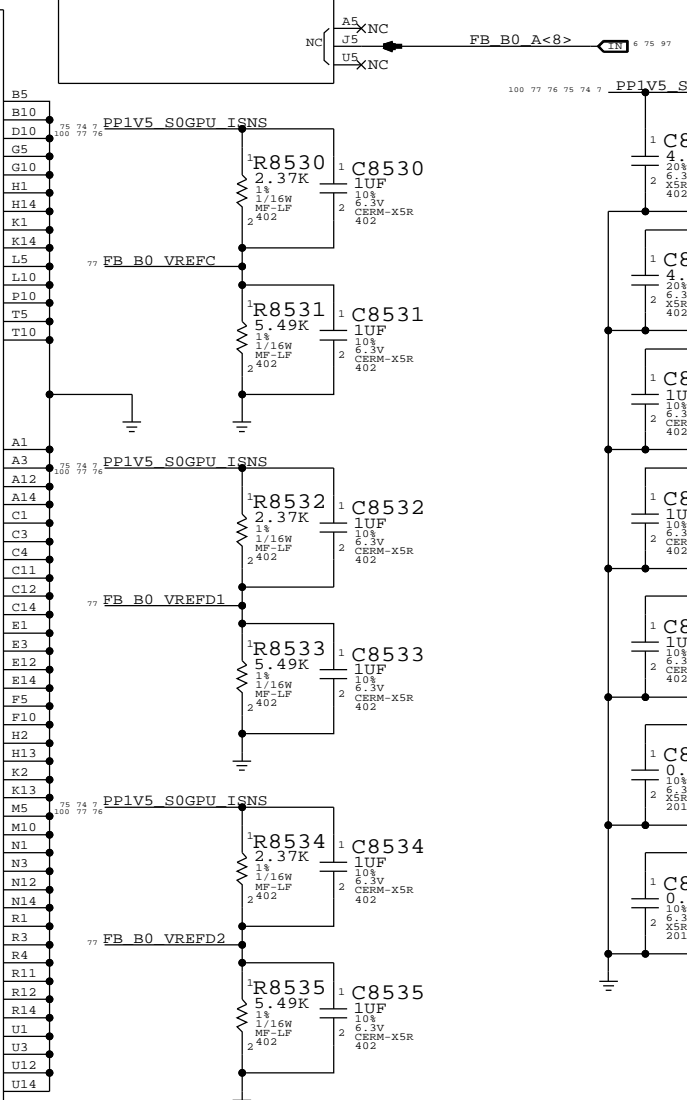
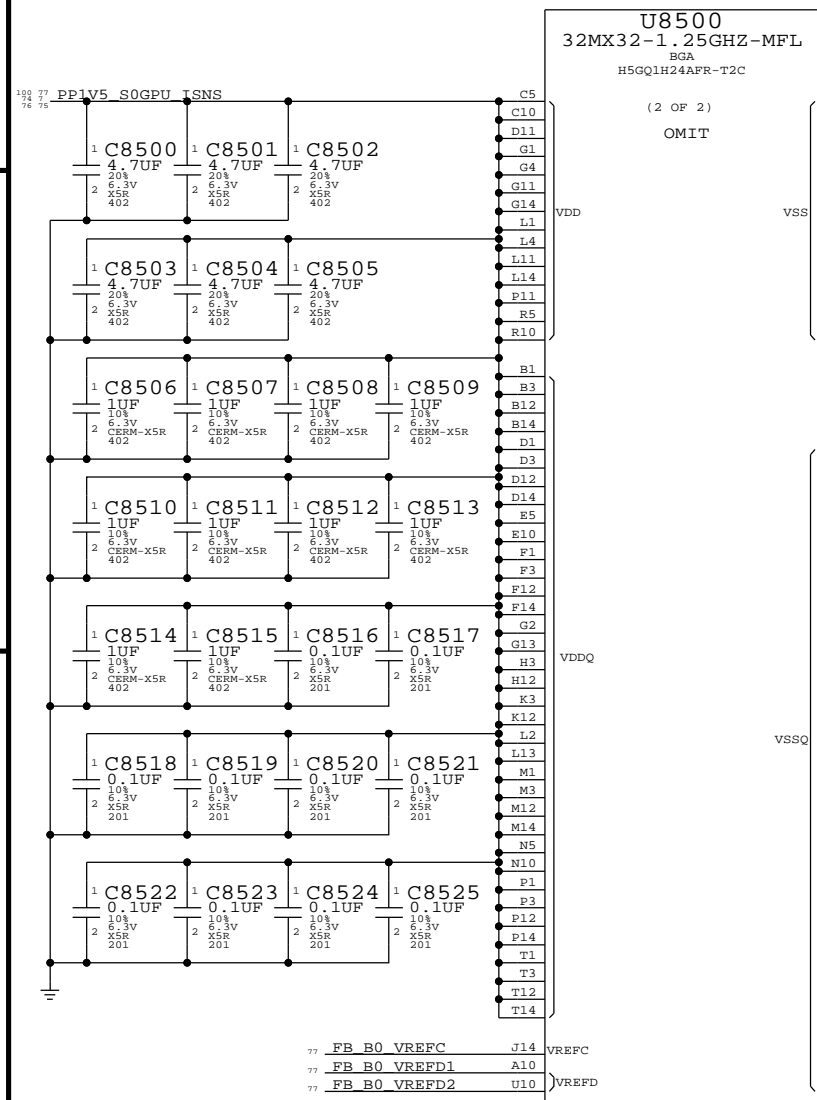
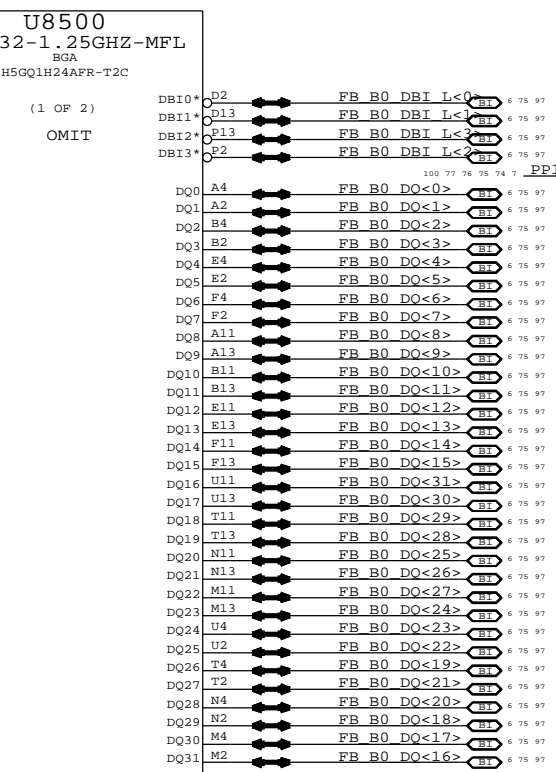
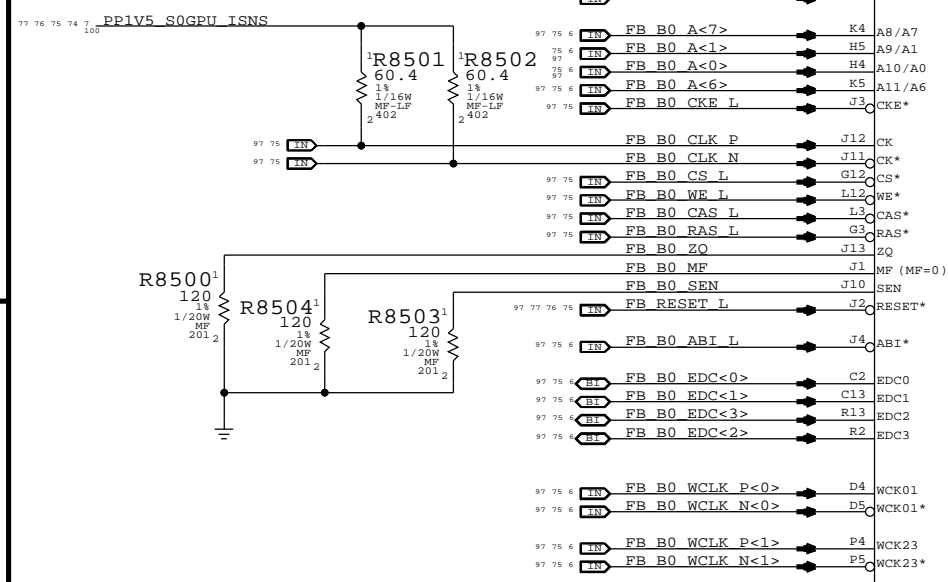
BOM options provided by this page:
(NONE)

D

C

B

A



D

C

B

A

SYNC MASTER=K92_MLB SYNC DATE=08/19/2010

GDDR5 Frame Buffer B

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VRAM BOM OPTION TABLE

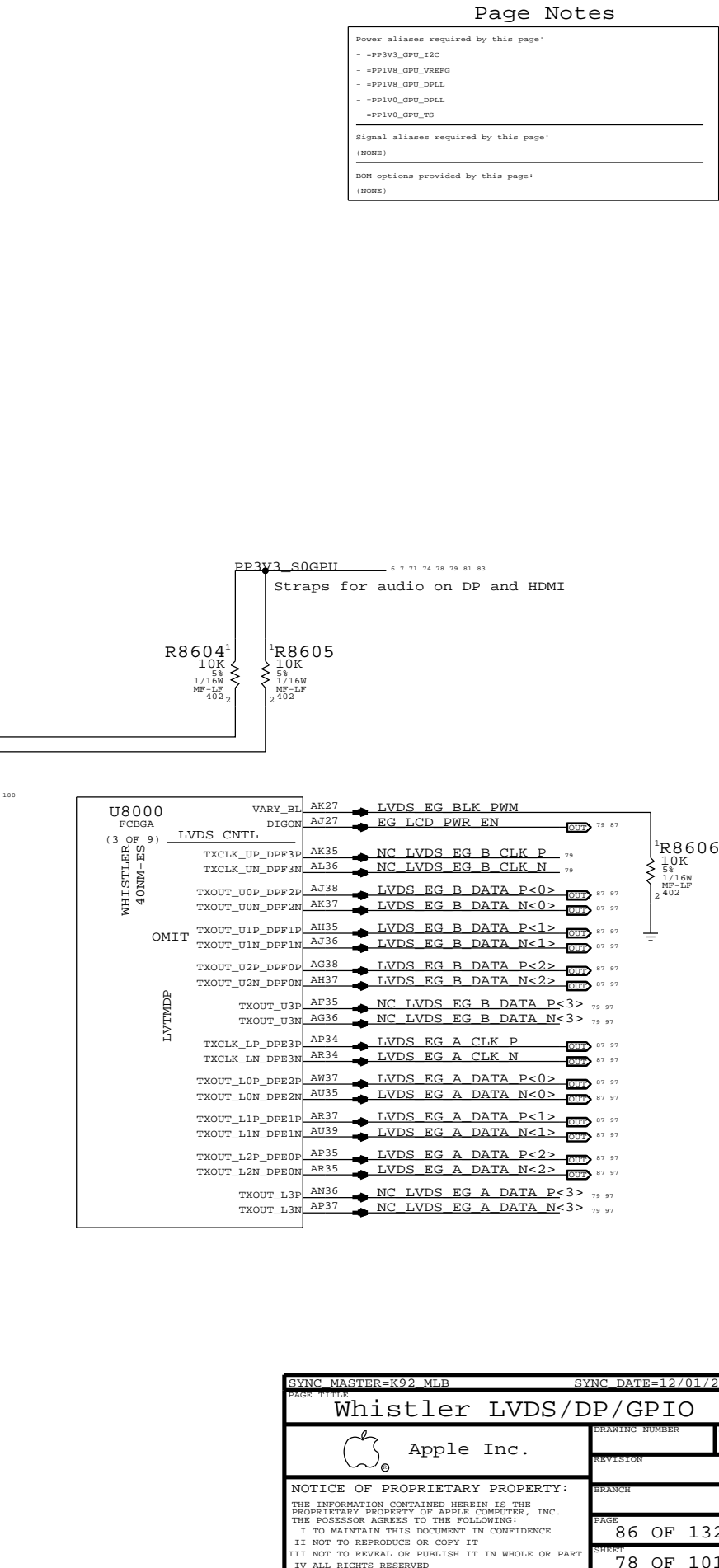
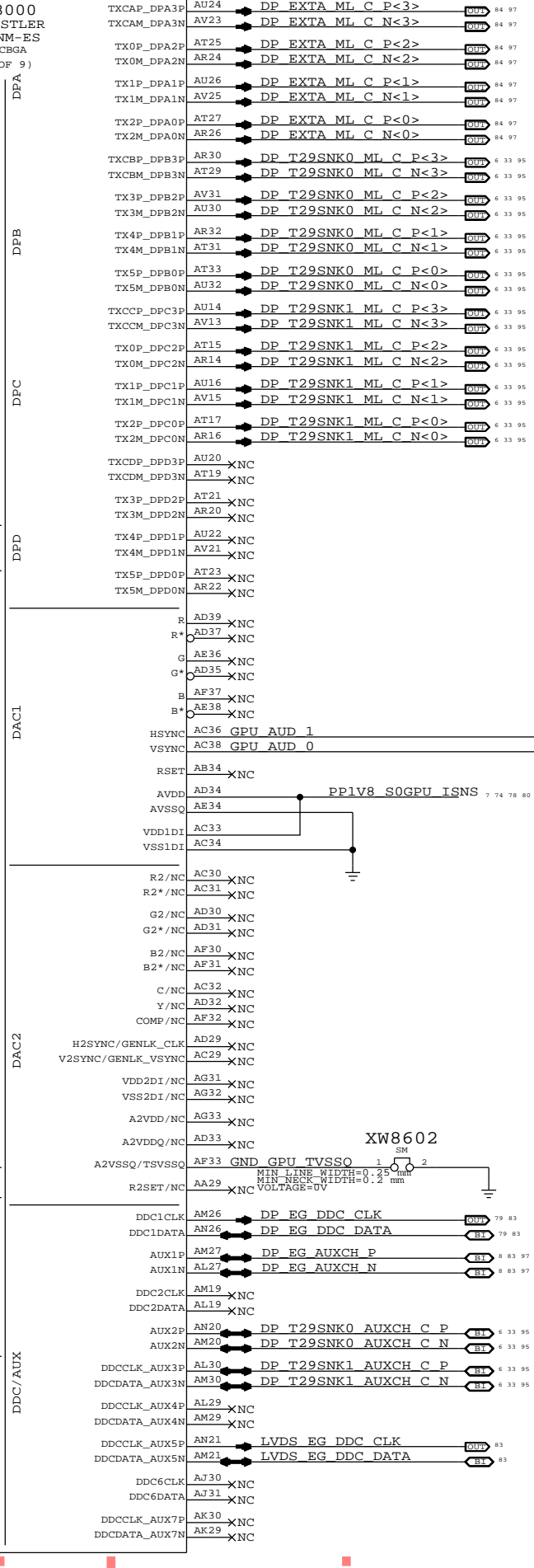
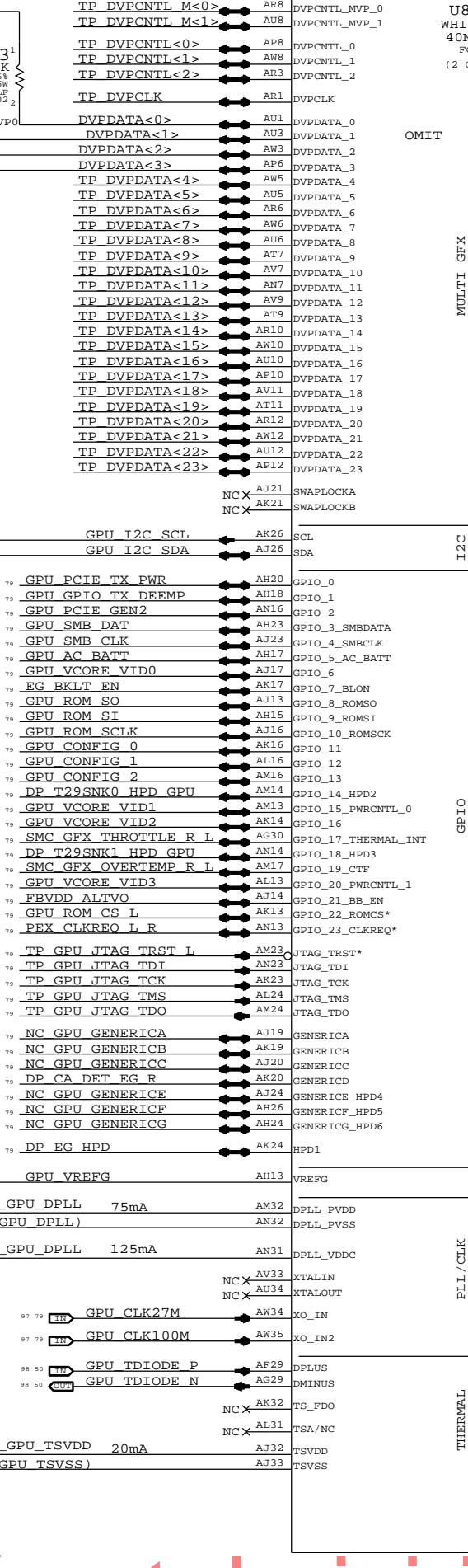
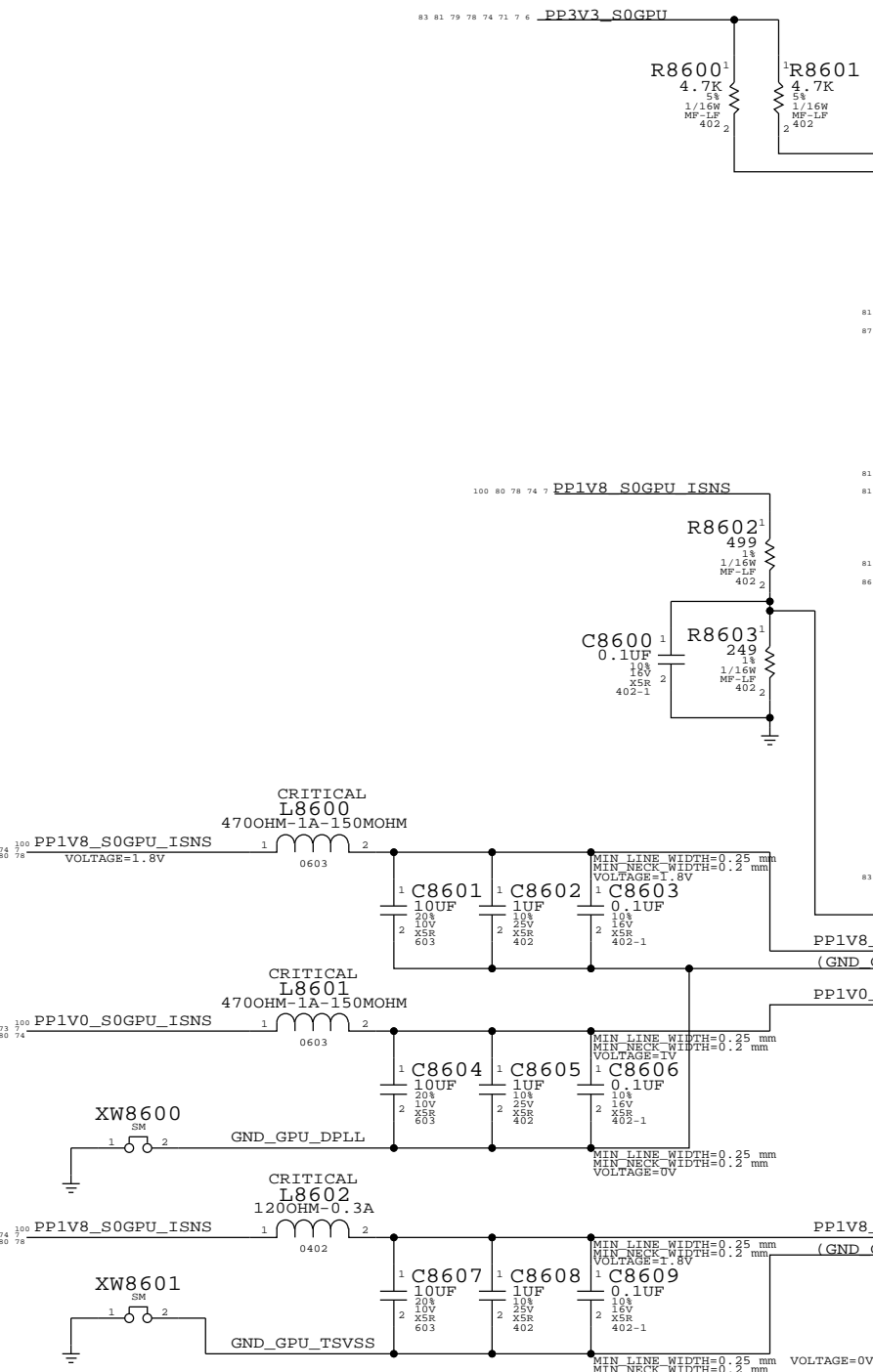
	VRAM_DVP0 (STUFF R8613?)	VRAM_DVP1 (STUFF R8612?)	VRAM_DVP2 (STUFF R8611?)
K92 SAMSUNG 1G	NO	NO	YES
K92 HYNIX 1G	YES	NO	YES
K91F SAMSUNG 512M	NO	NO	NO
K91F HYNIX 512M	NO	YES	NO
K91F SAMSUNG 1G	YES	NO	NO
K91F HYNIX 1G	YES	YES	NO

NOTE: AMD STRAPS FOR IDENTIFYING VRAM VENDOR & SIZE FOR WHISTLER

K92 Samsung 1G - NOSTUFF R8613, NOSTUFF R8612, STUFF R8611
K92 Hynix 1G - STUFF R8613, NOSTUFF R8612, STUFF R8611

K91FSamsung 512M - NOSTUFF R8613, NOSTUFF R8612, NOSTUFF R8611
K91FHynix 512M - NOSTUFF R8613, STUFF R8612, NOSTUFF R8611
K91FSamsung 1G - STUFF R8613, NOSTUFF R8612, NOSTUFF R8611
K91FHynix 1G - STUFF R8613, STUFF R8612, NOSTUFF R8611

NO STRAP CHANGES ARE REQUIRED FOR SEYMOUR BASED SYSTEMS



Page Notes

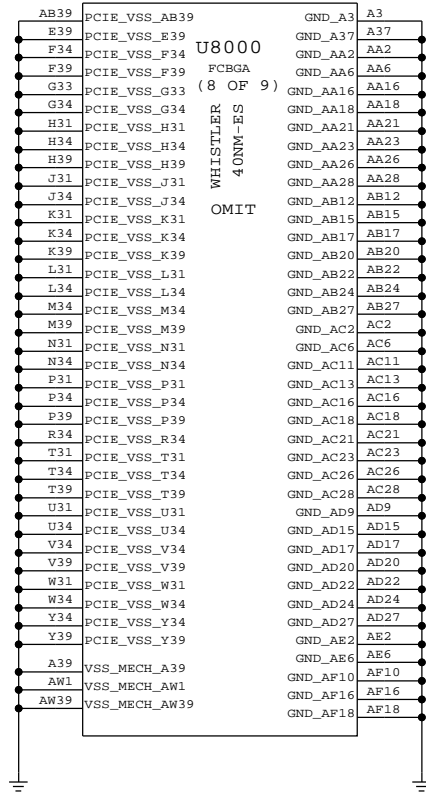
Power aliases required by this page:
- PP1V3_GPU_I2C
- PP1V8_GPU_VREFP
- PP1V8_GPU_DPLL
- PP1V0_GPU_DPLL
- PP1V0_GPU_TS

Signal aliases required by this page:
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BOM options provided by this page:
(NONE)

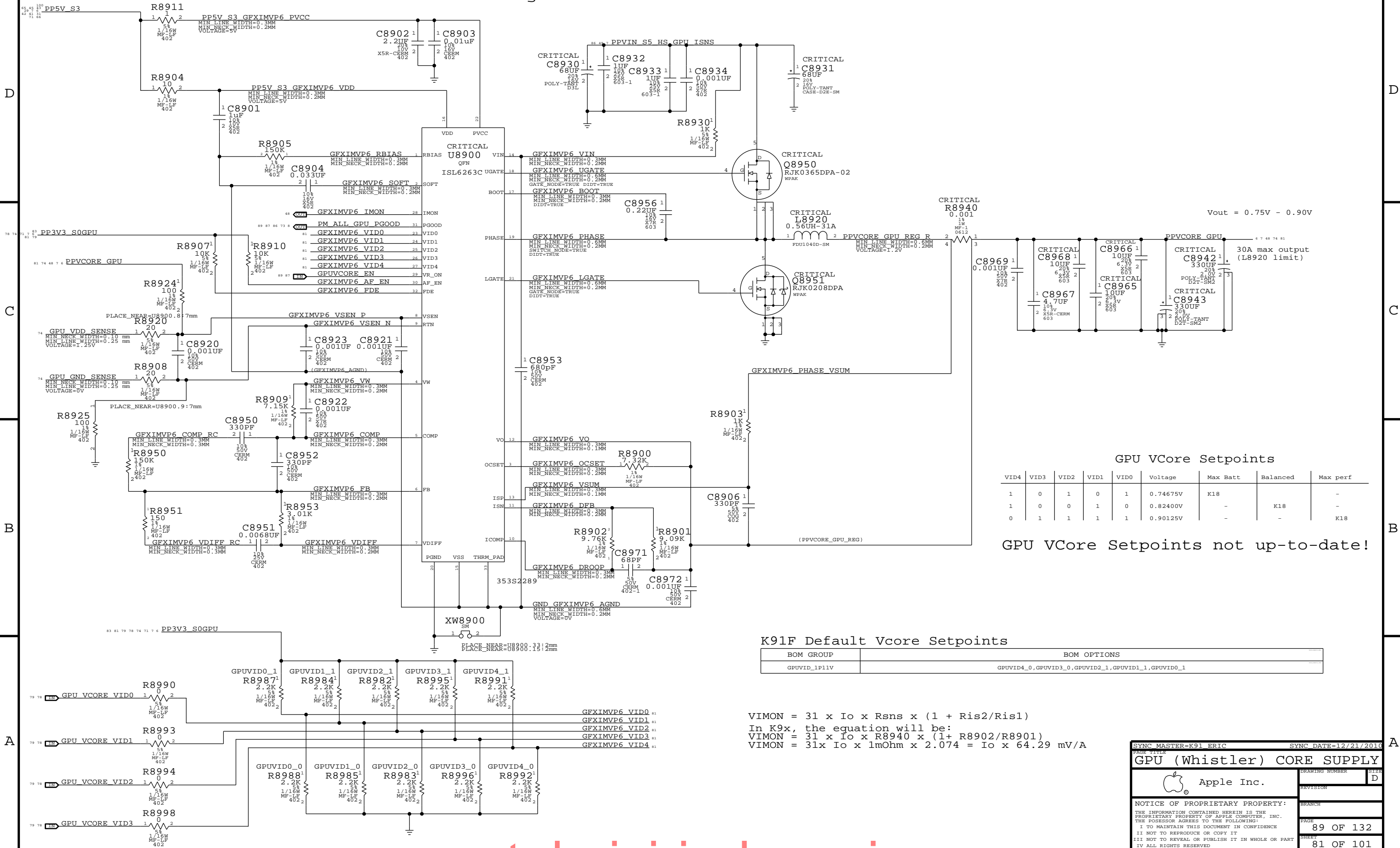
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AF21	GND_AF21	U8000	GND_F31	F31
AG2	GND_AG2	FCBGA	GND_F33	F33
AG6	GND_AG6	(9 OF 9)	GND_G2	G2
AG9	GND_AG9	WHISTLER	GND_G6	G6
AG17	GND_AG17	40NM-ES	GND_H9	H9
AG20	GND_AG20		GND_J2	J2
AG22	GND_AG22		GND_J6	J6
AH21	GND_AH21		GND_J8	J8
AJ2	GND_AJ2	OMIT	GND_J27	J27
AJ6	GND_AJ6		GND_K7	K7
AJ10	GND_AJ10		GND_K14	K14
AJ11	GND_AJ11		GND_L2	L2
AJ28	GND_AJ28		GND_L6	L6
AK7	GND_AK7		GND_L11	L11
AK11	GND_AK11		GND_L17	L17
AK31	GND_AK31		GND_L22	L22
AL2	GND_AL2		GND_L24	L24
AL6	GND_AL6		GND_M17	M17
AL8	GND_AL8		GND_M22	M22
AL11	GND_AL11		GND_M24	M24
AL14	GND_AL14		GND_N2	N2
AL17	GND_AL17		GND_N6	N6
AL20	GND_AL20		GND_N16	N16
AL23	GND_AL23		GND_N18	N18
AL26	GND_AL26		GND_N21	N21
AL32	GND_AL32		GND_N23	N23
AM9	GND_AM9		GND_N26	N26
AM11	GND_AM11		GND_R2	R2
AM31	GND_AM31		GND_R6	R6
AN2	GND_AN2		GND_R15	R15
AN6	GND_AN6		GND_R17	R17
AN8	GND_AN8		GND_R20	R20
AN11	GND_AN11		GND_R22	R22
AN30	GND_AN30		GND_R24	R24
AP7	GND_AP7		GND_R27	R27
AP9	GND_AP9		GND_T11	T11
AP11	GND_AP11		GND_T13	T13
AR5	GND_AR5		GND_T16	T16
B7	GND_B7		GND_T18	T18
B9	GND_B9		GND_T21	T21
B11	GND_B11		GND_T23	T23
B13	GND_B13		GND_T26	T26
B15	GND_B15		GND_U2	U2
B17	GND_B17		GND_U6	U6
B19	GND_B19		NC/GND	U13
B21	GND_B21		GND_U15	U15
B23	GND_B23		GND_U17	U17
B25	GND_B25		GND_U20	U20
B27	GND_B27		GND_U22	U22
B29	GND_B29		GND_U24	U24
B31	GND_B31		GND_U27	U27
B33	GND_B33		GND_V11	V11
C1	GND_C1		NC/GND	V13
C39	GND_C39		GND_V16	V16
E5	GND_E5		GND_V18	V18
E35	GND_E35		GND_V21	V21
F7	GND_F7		GND_V23	V23
F9	GND_F9		GND_V26	V26
F11	GND_F11		GND_W2	W2
F13	GND_F13		GND_W6	W6
F15	GND_F15		GND_Y15	Y15
F17	GND_F17		GND_Y17	Y17
F19	GND_F19		GND_Y20	Y20
F21	GND_F21		GND_Y22	Y22
F23	GND_F23		GND_Y24	Y24
F25	GND_F25		GND_Y27	Y27
F27	GND_F27		GND/PX_EN	AL21
F29	GND_F29			XNC

GPU VCore Regulator



GPU VCore Setpoints

VID4	VID3	VID2	VID1	VID0	Voltage	Max Batt	Balanced	Max perf
1	0	1	0	1	0.74675V	K18		-
1	0	0	1	0	0.82400V	-	K18	-
0	1	1	1	1	0.90125V	-	-	K18

GPU VCore Setpoints not up-to-date!

K91F Default Vcore Setpoints

BOM GROUP	BOM OPTIONS
GPUVID_1P11V	GPUVID4_0, GPUVID3_0, GPUVID2_1, GPUVID1_1, GPUVID0_1

VIMON = 31 x Io x Rsns x (1 + Ris2/Ris1)
In K9x, the equation will be:
VIMON = 31 x Io x R8940 x (1+ R8902/R8901)
VIMON = 31x Io x 1mOhm x 2.074 = Io x 64.29 mV/A

SYNC MASTER=K91.ERIC

SYNC DATE=12/21/2010

GPU (Whistler) CORE SUPPLY

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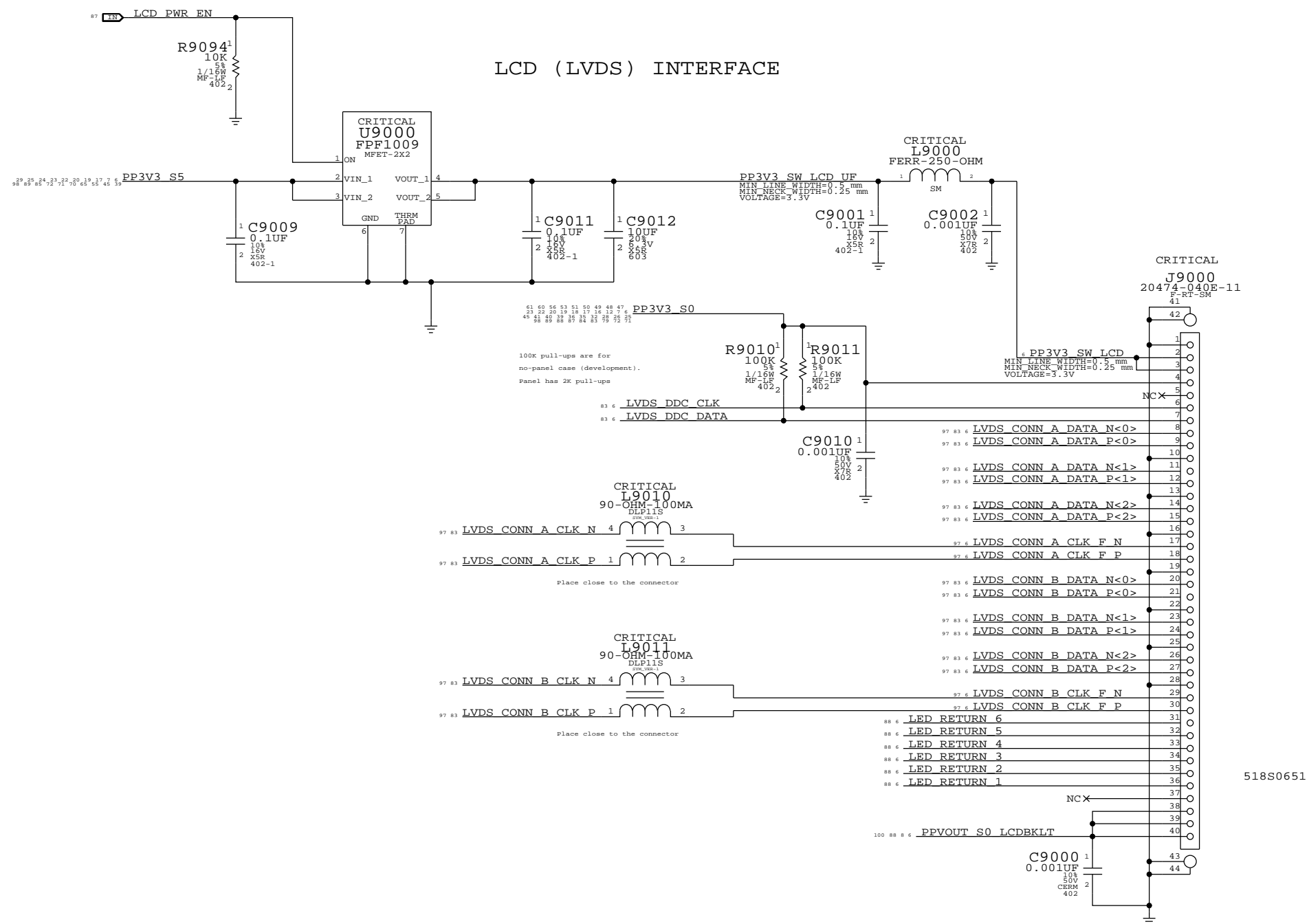
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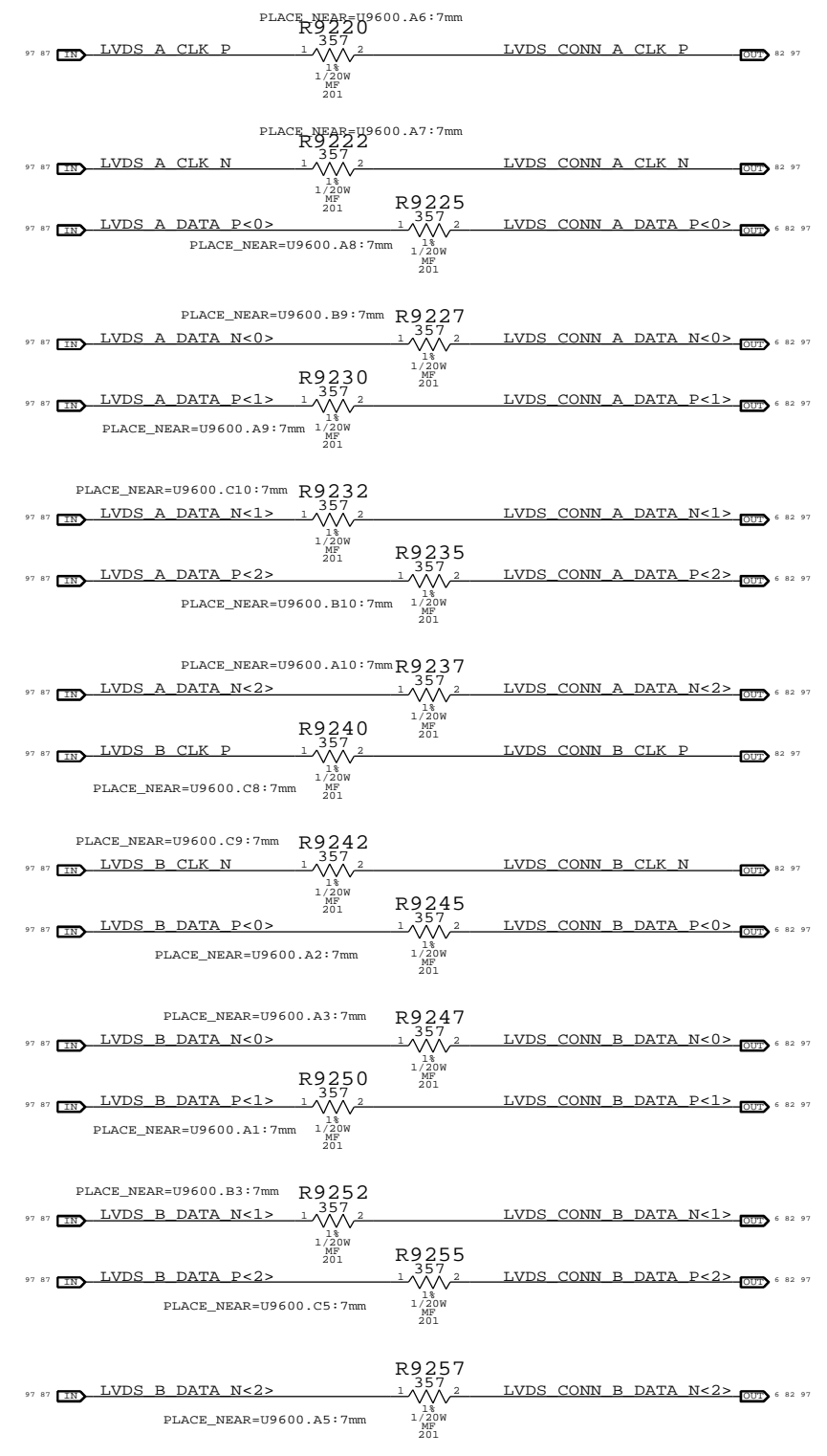
89 OF 132

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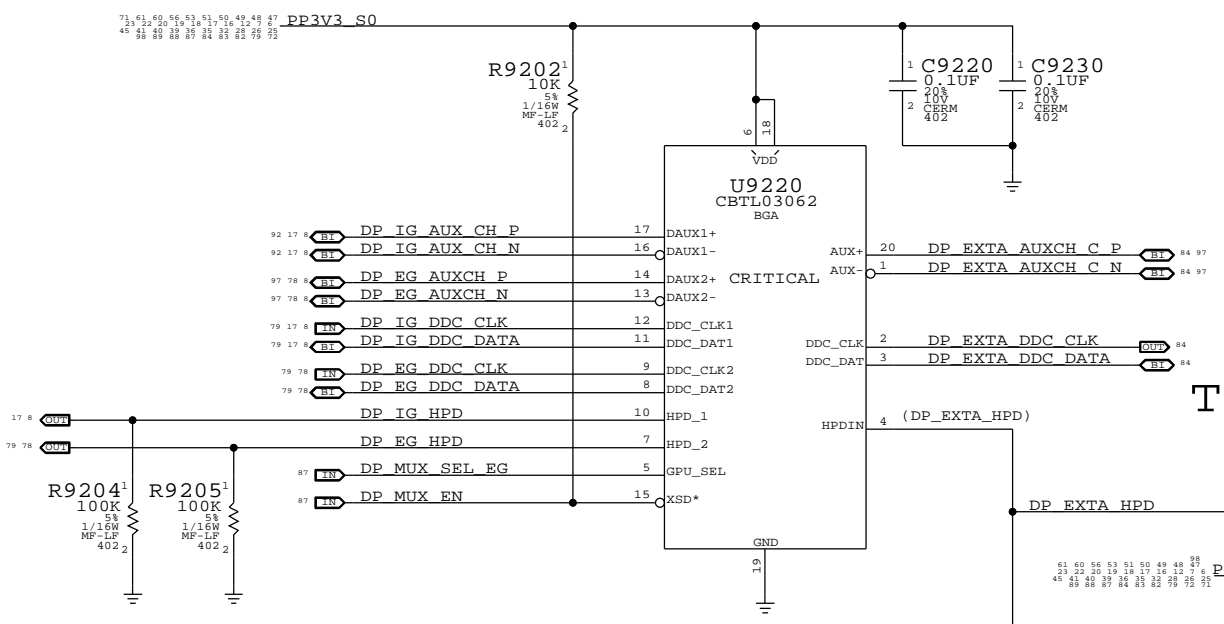


LVDS Transmitter Termination

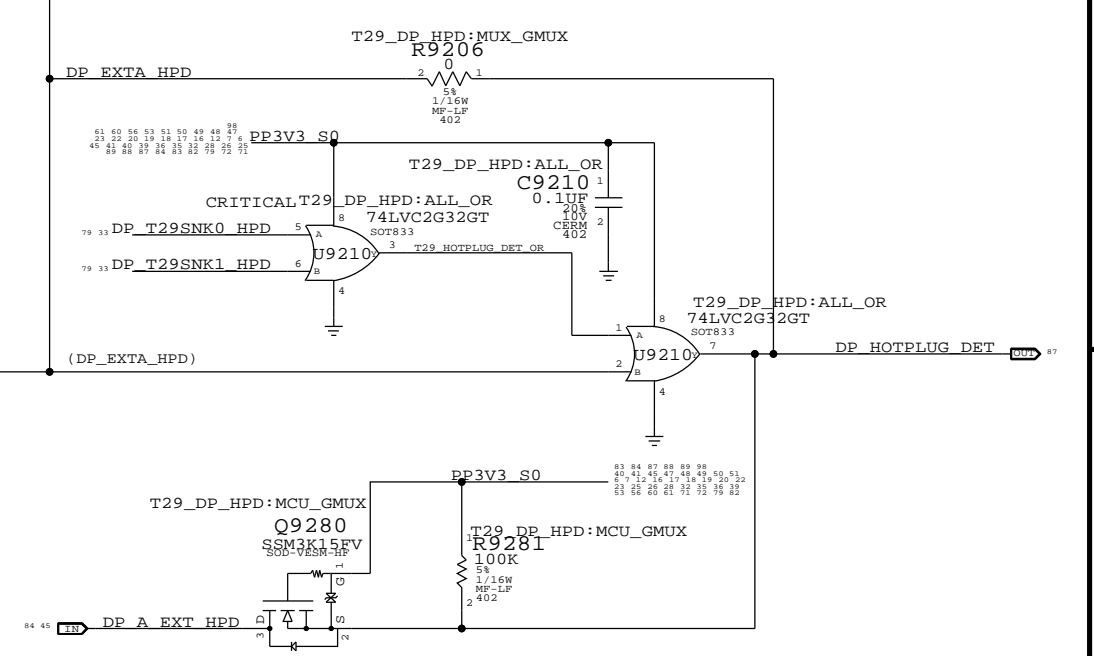
All emulated LVDS outputs require this termination



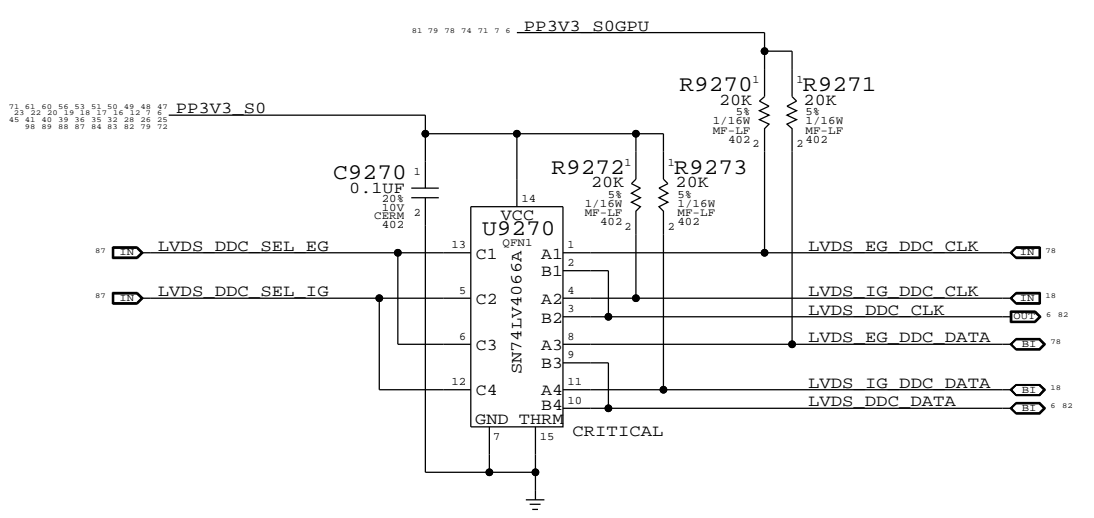
DP AUX, DDC, & HPD muxing to IG/EG



T29/DP HOT PLUG IN



LVDS DDC MUX



SYNC MASTER=K92 MLB

SYNC DATE=11/21/2010

Muxed Graphics Support

Apple Inc.

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```
A  =T29_WAKE_L:
    use PCIe WAKE#
```

R9330 provides pads for programming/debug of MCU, please make accessible.
If project has space for 10-pin programming header it should be used.

Note: U9390 ML/HPD defaults to T29 mode so that DP/T29 Display can detect host T29 support using I2C pull-ups on ML<3>. U9390 AUX defaults to DP mode because 100-ohm pull-downs would defeat DP Sink's detection of DP Source.

SYNC MASTER=T29 REF		SYNC DATE=10/16/2010	
PAGE TITLE			
DisplayPort/T29		A MUXing	
 Apple Inc.		DRAWING NUMBER	SIZE D
		REVISION	
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		SHEET	84 OF 101



D

C

B

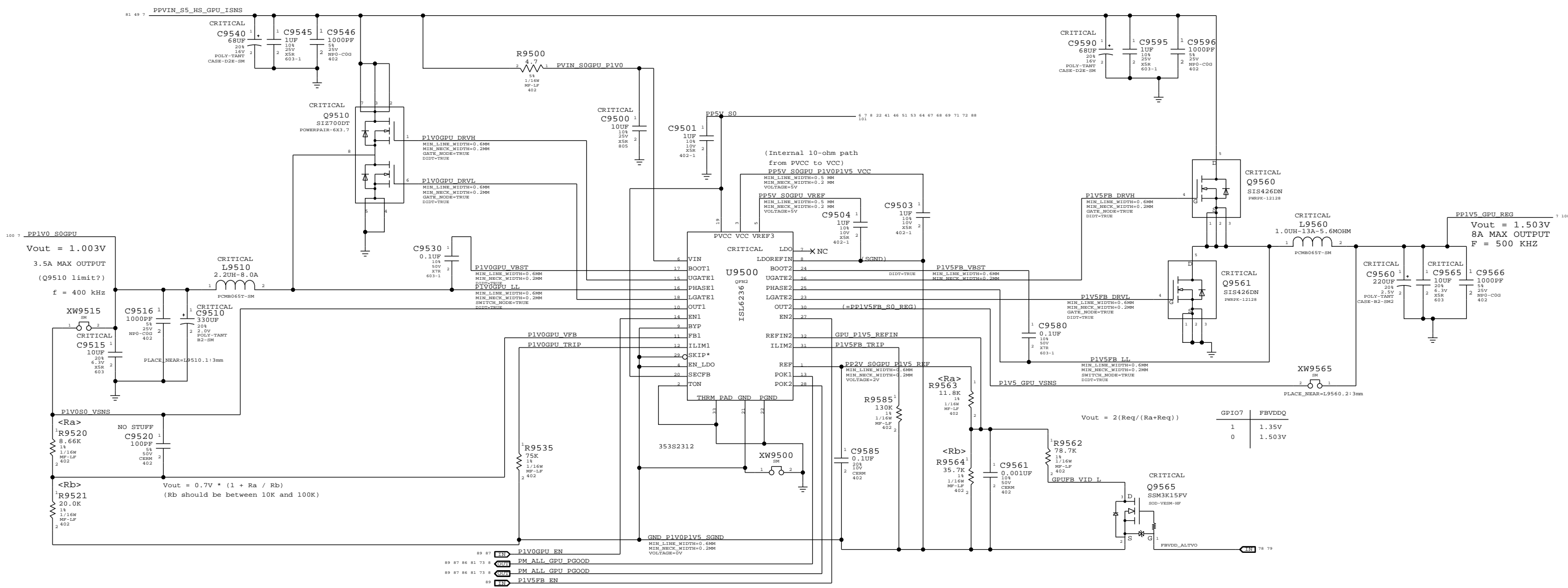
A

D

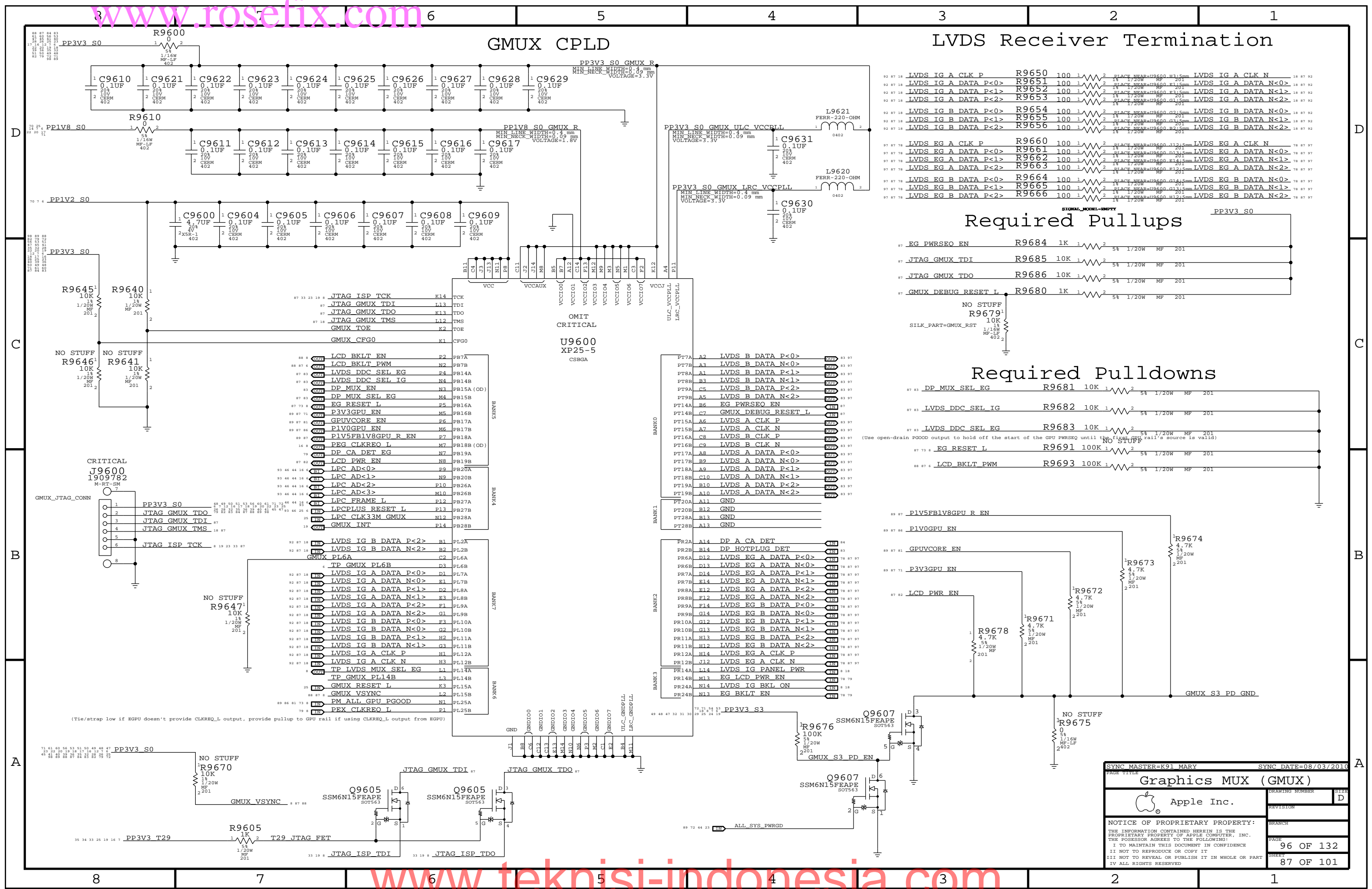
C

B

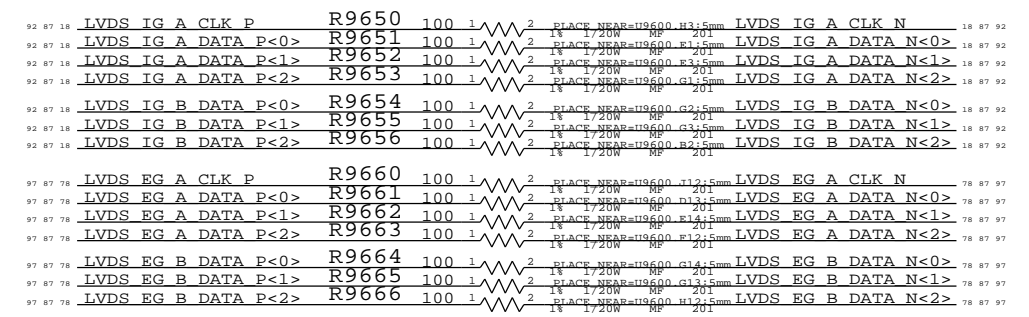
A



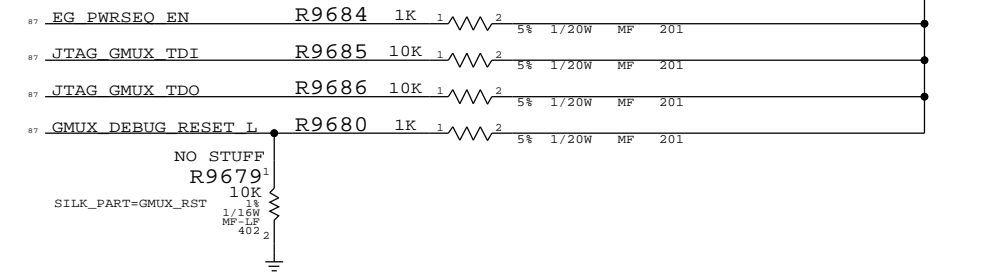
SYNC MASTER=K91.ERIC		SYNC DATE=10/08/2010	
PAGE TITLE		1V0 GPU / 1V5 FB Power Supply	
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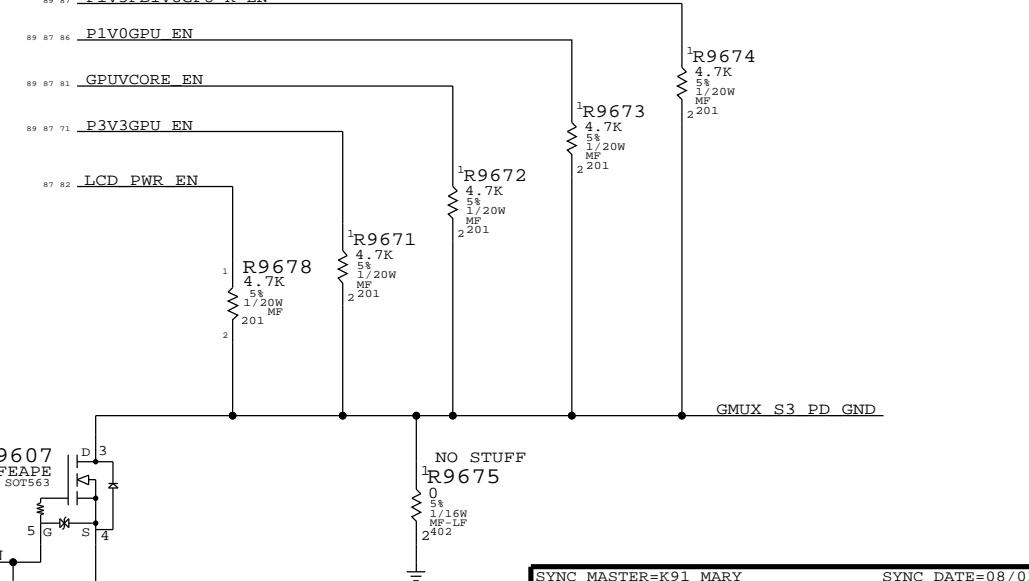
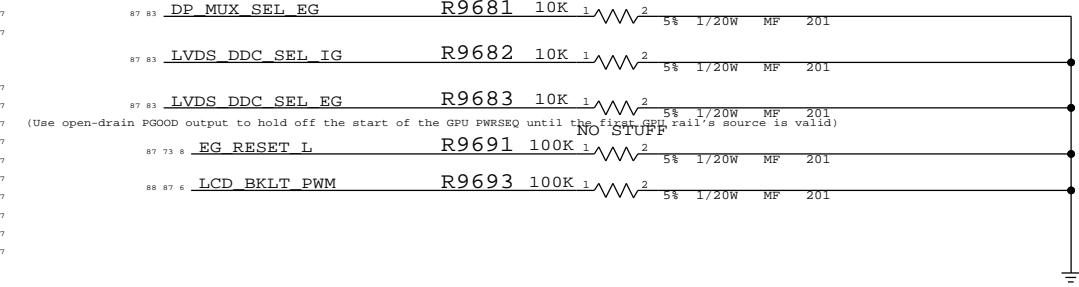
LVDS Receiver Termination



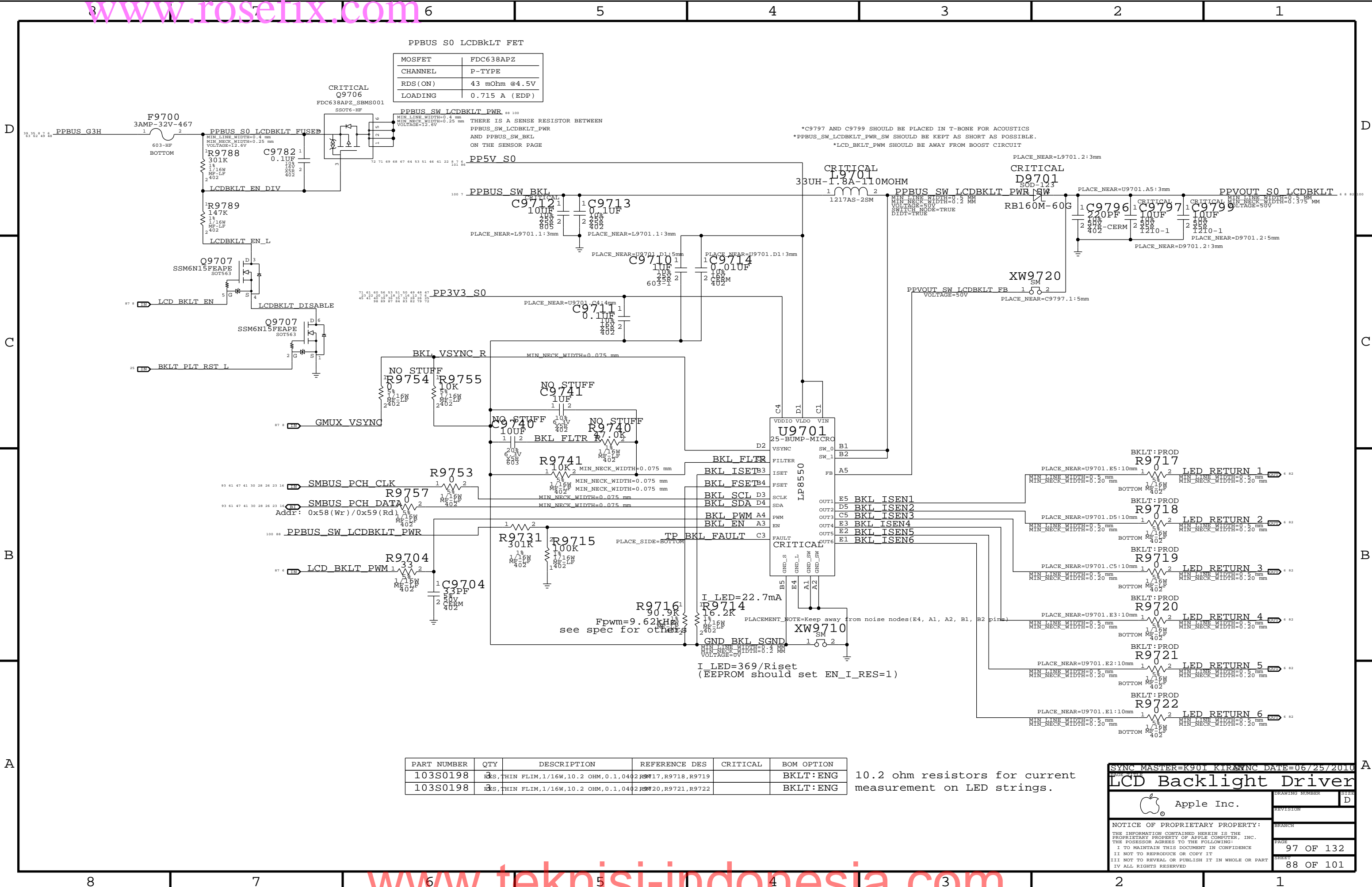
Required Pullups



Required Pulldowns



SYNC MASTER=K91 MARY		SYNC DATE=08/03/2010	
PAGE TITLE			
Graphics MUX (GMUX)		DRAWING NUMBER	SIZE D
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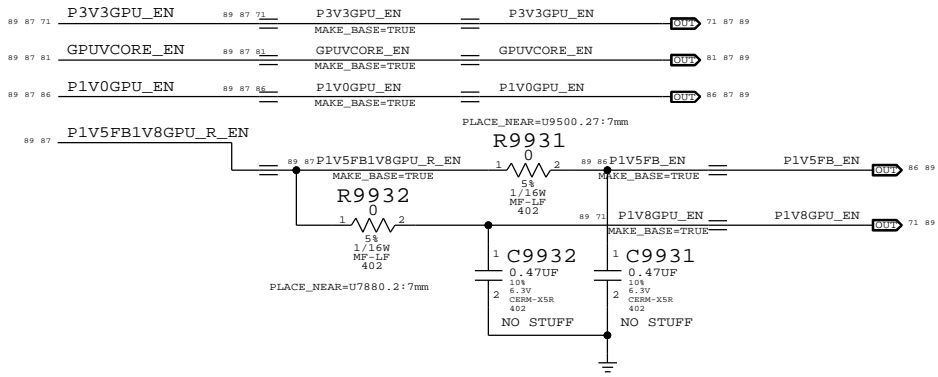
B

A

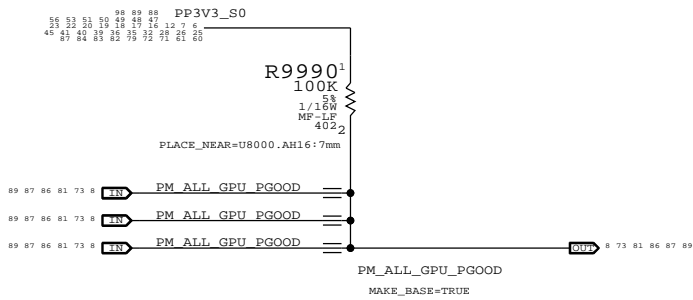
GPU Rail Sequencing

Whistler GPU requires rails to come up in the following order:

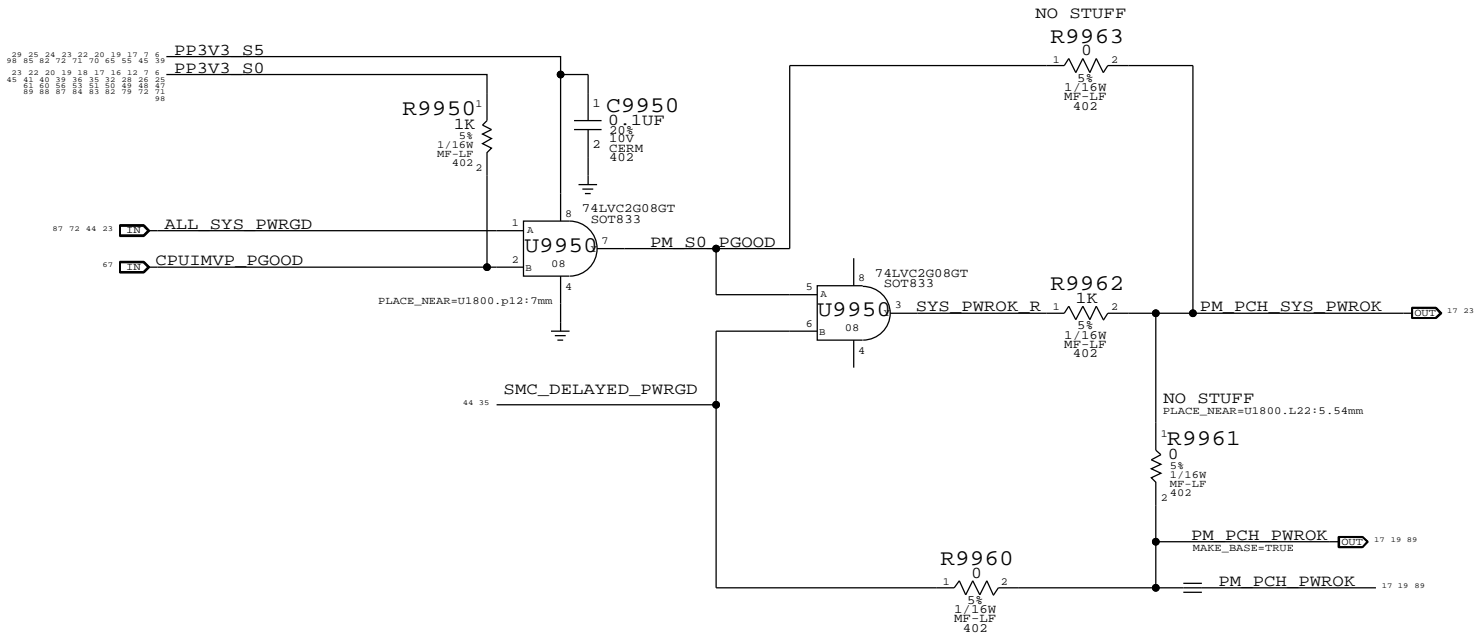
- 1) GPU_3.3V
- 2) GPUVcore
- 3) GPU_1.0V
- 4) GPU_1.8V/GDDR5 1.5/1.35V



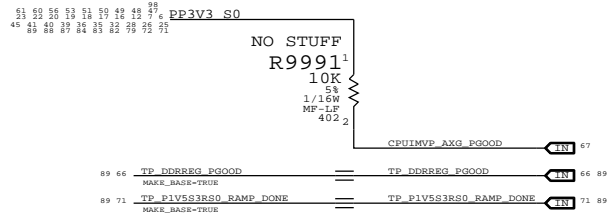
EXT GPU PWRGD Pullup



PCH S0 PWRGD



Unused PGOOD signal



SYNC MASTER=K91 MARY		SYNC DATE=08/03/2010	
PAGE TITLE		Power Sequencing EG/PCH S0	
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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	20 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_VID	*	0.457 MM	?

Most CPU signals with impedance requirements are 50-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: Calpella SFF DG (DG-407364_v1.5), Section 2.8

PCI-Express


PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

CPU Net Properties

		NET_TYPE	
ELECTRICAL_CONSTRAINT_SET		PHYSICAL	SPACING
DMI_S2N	PCIE_85D	PCIE	DMI_S2N P<3:0>
DMI_S2N	PCIE_85D	PCIE	DMI_S2N N<3:0>
DMI_N2S	PCIE_85D	PCIE	DMI_N2S P<3:0>
DMI_N2S	PCIE_85D	PCIE	DMI_N2S N<3:0>
FDI_DATA	PCIE_85D	PCIE	FDI_DATA P<7:0>
FDI_DATA	PCIE_85D	PCIE	FDI_DATA N<7:0>
	CPU_50S	CPU_AGTL	FDI_FSYNC<1..0>
	CPU_50S	CPU_AGTL	FDI_LSYNC<1..0>
DMI_CLK100M	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_P
	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_N
	CPU_50S	CPU_AGTL	FDI_INT
CPU_PECT	CPU_50S	PCIE	CPU_PECI
PM_SYNC	CPU_50S	CPU_AGTL	PM_SYNC
PM_MEM_PWRGD	CPU_50S	CPU_AGTL	PM_MEM_PWRGD
XDP_CPU_PWRGOOD	CPU_50S	CPU_ITP	XDP_CPU_PWRGD
XDP_DBRESET_L	CPU_50S	CPU_ITP	XDP_DBRESET_L
XDP_PRDY_L	CPU_50S	CPU_ITP	XDP_CPU_PRDY_L
XDP_PREQ_L	CPU_50S	CPU_ITP	XDP_CPU_PREQ_L
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP0
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP1
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP2
CPU_CFG	CPU_50S	CPU_ITP	CPU_CFG<11..0>
CPU_CFG	CPU_50S	CPU_ITP	CPU_CFG<17..16>
CPU_CATERR_L	CPU_50S	CPU_AGTL	CPU_CATERR_L
	CPU_50S	CPU_AGTL	CPU_PROC_SEL_L
	CPU_50S	CPU_AGTL	TP_CPU_VTT_SELECT
CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU_PROCHOT_L
CPU_PWRGD	CPU_50S	CPU_AGTL	CPU_PWRGD
PM_THRMTRIP_L	CPU_50S	CPU_8MIL	PM_THRMTRIP_L
XDP_CLK_CPU	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M_P
XDP_CLK_CPU	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M_N
XDP_CLK_PCH	CLK_PCIE_90D	CLK_PCIE	ITPXDP_CLK100M_P
XDP_CLK_PCH	CLK_PCIE_90D	CLK_PCIE	ITPXDP_CLK100M_N
XDP_CLK_ITP	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_P
XDP_CLK_ITP	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_N
PM_DPRSLEVR	CPU_55S	CPU_8MIL	CPU_PSI_L
	CPU_50S	CPU_AGTL	PM_DPRSLEVR
	CPU_27P4S	CPU_COMP	CPU_PEG_COMP
	CPU_27P4S	CPU_COMP	CPU_PEG_RBIA5
	CPU_27P4S	CPU_COMP	CPU_COMP3
	CPU_27P4S	CPU_COMP	CPU_COMP2
	CPU_27P4S	CPU_COMP	CPU_COMP1
	CPU_27P4S	CPU_COMP	CPU_COMP0
XDP_TDI	CPU_50S	CPU_ITP	XDP_CPU_TDI
XDP_TDO	CPU_50S	CPU_ITP	XDP_CPU_TDO
XDP_TMS	CPU_50S	CPU_ITP	XDP_CPU_TMS
XDP_TCK	CPU_50S	CPU_ITP	XDP_CPU_TCK
XDP_TEST_L	CPU_50S	CPU_ITP	XDP_CPU_TRST_L
XDP_BPM	CPU_50S	CPU_ITP	XDP_BPM_L<3..0>
XDP_BPM_L	CPU_50S	CPU_ITP	XDP_BPM_L<7..4>
(FSB_CPURST_L)	CPU_50S	CPU_ITP	XDP_CPURST_L
	CPU_55S	CPU_8MIL	CPU_VID<6..0>
	CPU_50S	CPU_AGTL	CPUIMVP_IMON
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCIOSENSE_P
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCIOSENSE_N
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_SENSE_P
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_SENSE_N
	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_P
	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_N
	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_P
	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_N
PM_DPRSLEVR	CPU_55S	CPU_8MIL	GFX_VID<6..0>
	CPU_50S	CPU_AGTL	GFX_DPRSLEVR
	CPU_50S	CPU_AGTL	GFX_VR_EN
	CPU_50S	CPU_AGTL	GFXIMVP_IMON
	PCIE_85D	PCIE	PEG_R2D_P<7..0>
	PCIE_85D	PCIE	PEG_R2D_N<7..0>
PEG_R2D	PCIE_85D	PCIE	PEG_R2D_C_P<7..0>
	PCIE_85D	PCIE	PEG_R2D_C_N<7..0>
PEG_D2R	PCIE_85D	PCIE	PEG_D2R_P<7..0>
	PCIE_85D	PCIE	PEG_D2R_N<7..0>
	PCIE_85D	PCIE	PEG_D2R_C_P<7..0>
	PCIE_85D	PCIE	PEG_D2R_C_N<7..0>
	CPU_50S	CPU_VID	CPU_VIDSOUT
	CPU_50S	CPU_VID	CPU_VIDCLK
	CPU_50S	CPU_VID	CPU_VIDALERT_L

SYNC_MASTER=K92_MLB		SYNC_DATE=08/09/2010	
PAGE TITLE		CPU Constraints	
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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_37S	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=STANDARD	=STANDARD
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=3:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_20OTHER	*	25 MILS	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_20OTHER
MEM_CTRL	*	*	MEM_20OTHER
MEM_CMD	*	*	MEM_20OTHER
MEM_DATA	*	*	MEM_20OTHER
MEM_DQS	*	*	MEM_20OTHER

DDR3:

DQ/DM signals should be matched within 0.508mm of associated DQS pair.

DQS intra-pair matching should be within 0.127mm, no inter-pair matching requirement.

DQS to clock matching should be within [CLK-12.7mm] and [CLK+25.4mm].

CLK intra-pair matching should be within 0.127mm, inter-pair matching should be within 0.508mm.

CONTROL signals should be matched within [CLK-12.7mm] to [CLK+0.0mm] of CLK pairs.

A/BA/CMD signals should be matched within [CLK-12.7mm] to [CLK+12.7mm] of CLK pairs.


DQ/DQS/A/BA/cmd signal spacing is 4x dielectric, CLK is 5x dielectric.

Maximum length of any signal from die pad to SODIMM pad is 139.7mm, from procesor ball to SODIMM pad is 114.3mm.













SOURCE: Calpella SFF Platform DG, Rev 1.5 (#407364), Section 2.2

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
MEM_A_CLK	MEM_72D	MEM_CLK	MEM A CLK P<5..0>	6 11 26
MEM_A_CLK	MEM_72D	MEM_CLK	MEM A CLK N<5..0>	6 11 26
MEM_A_CNTRL	MEM_37S	MEM_CTRL	MEM A CKE<3..0>	6 11 26
MEM_A_CNTRL	MEM_37S	MEM_CTRL	MEM A CS L<3..0>	6 11 26
MEM_A_CNTRL	MEM_37S	MEM_CTRL	MEM A ODT<3..0>	6 11 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A A<15..0>	6 11 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A BA<2..0>	6 11 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A RAS L	6 11 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A CAS L	6 11 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A WE L	6 11 26
MEM_A_DQ_BYTE0	MEM_50S	MEM_DATA	MEM A DQ<7..0>	6 11 27
MEM_A_DQ_BYTE1	MEM_50S	MEM_DATA	MEM A DQ<15..8>	6 11 27
MEM_A_DQ_BYTE2	MEM_50S	MEM_DATA	MEM A DQ<23..16>	6 11 27
MEM_A_DQ_BYTE3	MEM_50S	MEM_DATA	MEM A DQ<31..24>	6 11 27
MEM_A_DQ_BYTE4	MEM_50S	MEM_DATA	MEM A DQ<39..32>	6 11 26 27
MEM_A_DQ_BYTE5	MEM_50S	MEM_DATA	MEM A DQ<47..40>	6 11 27
MEM_A_DQ_BYTE6	MEM_50S	MEM_DATA	MEM A DQ<55..48>	6 11 27
MEM_A_DQ_BYTE7	MEM_50S	MEM_DATA	MEM A DQ<63..56>	6 11 27
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM A DQS P<0>	6 11 27
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM A DQS N<0>	6 11 27
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM A DQS P<1>	6 11 27
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM A DQS N<1>	6 11 27
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM A DQS P<2>	6 11 27
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM A DQS N<2>	6 11 27
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM A DQS P<3>	6 11 27
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM A DQS N<3>	6 11 27
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM A DQS P<4>	6 11 27
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM A DQS N<4>	6 11 27
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM A DQS P<5>	6 11 27
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM A DQS N<5>	6 11 27
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM A DQS P<6>	6 11 26 27
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM A DQS N<6>	6 11 26 27
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM A DQS P<7>	6 11 27
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM A DQS N<7>	6 11 27
MEM_B_CLK	MEM_72D	MEM_CLK	MEM B CLK P<5..0>	6 11 28
MEM_B_CLK	MEM_72D	MEM_CLK	MEM B CLK N<5..0>	6 11 28
MEM_B_CNTRL	MEM_37S	MEM_CTRL	MEM B CKE<3..0>	6 11 28
MEM_B_CNTRL	MEM_37S	MEM_CTRL	MEM B CS L<3..0>	6 11 28
MEM_B_CNTRL	MEM_37S	MEM_CTRL	MEM B ODT<3..0>	6 11 28
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B A<15..0>	6 11 28
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B BA<2..0>	6 11 28
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B RAS L	6 11 28
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B CAS L	6 11 28
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B WE L	6 11 28
MEM_B_DQ_BYTE0	MEM_50S	MEM_DATA	MEM B DQ<7..0>	6 11 27
MEM_B_DQ_BYTE1	MEM_50S	MEM_DATA	MEM B DQ<15..8>	6 11 27
MEM_B_DQ_BYTE2	MEM_50S	MEM_DATA	MEM B DQ<23..16>	6 11 27
MEM_B_DQ_BYTE3	MEM_50S	MEM_DATA	MEM B DQ<31..24>	6 11 27
MEM_B_DQ_BYTE4	MEM_50S	MEM_DATA	MEM B DQ<39..32>	6 11 27 28
MEM_B_DQ_BYTE5	MEM_50S	MEM_DATA	MEM B DQ<47..40>	6 11 27
MEM_B_DQ_BYTE6	MEM_50S	MEM_DATA	MEM B DQ<55..48>	6 11 27
MEM_B_DQ_BYTE7	MEM_50S	MEM_DATA	MEM B DQ<63..56>	6 11 27
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM B DQS P<0>	6 11 27
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM B DQS N<0>	6 11 27
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM B DQS P<1>	6 11 27
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM B DQS N<1>	6 11 27
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM B DQS P<2>	6 11 27
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM B DQS N<2>	6 11 27
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM B DQS P<3>	6 11 27
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM B DQS N<3>	6 11 27
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM B DQS P<4>	6 11 27
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM B DQS N<4>	6 11 27
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM B DQS P<5>	6 11 27
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM B DQS N<5>	6 11 27
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM B DQS P<6>	6 11 27 28
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM B DQS N<6>	6 11 27 28
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM B DQS P<7>	6 11 27
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM B DQS N<7>	6 11 27

SYNC MASTER=K18 MLB		SYNC DATE=04/27/2010	
PAGE TITLE			
Memory Constraints		DRAWING NUMBER	SIZE
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		BRANCH	
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Ethernet Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE			
		PHYSICAL	SPACING		
		ENET_50R	ENET_3Y	BCM5764 CLK25M XTALI	
		ENET_50R	ENET_3Y	BCM5764 CLK25M XTALO	
		ENET_50R	ENET_3Y	ENET RESET L	32 36
	ENET_MGT	ENET_MGT		ENET MDI P<3...0>	36 37
		ENET_100D	ENET_MDI	ENET MDI N<3...0>	36 37
		ENET_50R	ENET_CR	SDCONN DATA R<7...0>	
	CR_DATA_A0	ENET_50R	ENET_CR	SDCONN CMD R	32
	CR_DATA_A0	ENET_50R	ENET_CR	SDCONN CLK R	32
	CR_CLK	ENET_50R	ENET_CR	SDCONN DATA<7...0>	32 36
	CR_DATA_A0	ENET_50R	ENET_CR	SDCONN CMD	32 36
	CR_DATA_A0	ENET_50R	ENET_CR	SDCONN CLK	32 36
	CR_CLK	ENET_50R	ENET_CR	SDCONN CLK R L 32	

SOURCE: Broadcom 5764-DS04-RDS Page 38

SOURCE: Attila Farkas Email - 8/2/10











FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE			
		PHYSICAL	SPACING		
FW00	FW_E0_TPA	FW_110G	FW_TD	NC FW0 TPAP	6 38
FW05	FW_E0_TPA	FW_110G	FW_TD	NC FW0 TPAN	38 40
FW00	FW_E0_TPB	FW_110G	FW_TD	NC FW0 TPBP	6 38
FW05	FW_E0_TPB	FW_110G	FW_TD	NC FW0 TPBN	6 38
FW00	FW_E1_TPA	FW_110G	FW_TD	FW PORT1 TPA P	38 40
FW05	FW_E1_TPA	FW_110G	FW_TD	FW PORT1 TPA N	38 40
FW00	FW_E1_TPB	FW_110G	FW_TD	FW PORT1 TPB P	38 40
FW05	FW_E1_TPB	FW_110G	FW_TD	FW PORT1 TPB N	38 40
Port 2 Not Used					





SOURCE: Broadcom 5764-DS04-RDS Page 38

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
 SMBUS_SMC_A_S3_SCL	SMB_50S	SMB	SMBUS_SMC_A_S3_SCL 6 31 44 47 53 54
 SMBUS_SMC_A_S3_SDA	SMB_50S	SMB	SMBUS_SMC_A_S3_SDA 6 31 44 47 53 54
 SMBUS_SMC_B_S0_SCL	SMB_50S	SMB	SMBUS_SMC_B_S0_SCL 44 47 50
 SMBUS_SMC_B_S0_SDA	SMB_50S	SMB	SMBUS_SMC_B_S0_SDA 44 47 50
 SMBUS_SMC_0_S0_SCL	SMB_50S	SMB	SMBUS_SMC_0_S0_SCL 6 31 44 47 50 79
 SMBUS_SMC_0_S0_SDA	SMB_50S	SMB	SMBUS_SMC_0_S0_SDA 6 31 44 47 50 79
 SMBUS_SMC_BSA_SCL	SMB_50S	SMB	SMBUS_SMC_BSA_SCL 6 44 47 62 63
 SMBUS_SMC_BSA_SDA	SMB_50S	SMB	SMBUS_SMC_BSA_SDA 6 44 47 62 63
 SMBUS_SMC_MGMT_SCL	SMB_50S	SMB	SMBUS_SMC_MGMT_SCL 44 47 100
 SMBUS_SMC_MGMT_SDA	SMB_50S	SMB	SMBUS_SMC_MGMT_SDA 44 47 100

SMBus Charger Net Properties


NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
 CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P 63
 CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_N 63
 CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P 63
 CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_N 63

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SYNC_DATE=04/27/2010

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SMC Constraints

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GDDR5 Frame Buffer Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR5_45R50SE	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	12.7 MM	=STANDARD	=STANDARD
GDDR5_45SE	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
GDDR5_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR5_CLK	*	=5x_DIELECTRIC	?
GDDR5_CMD	*	=2x_DIELECTRIC	?
GDDR5_DATA	*	=3x_DIELECTRIC	?
GDDR5_EDC	*	=7x_DIELECTRIC	?

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
LVDS_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?	DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?	LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 0.127 mm. Pairs should be within 0.508mm of entire channel.
DisplayPort/TMDS intra-pair matching should be 0.127mm. Inter-pair matching should be within 2.54cm. Max Length 241.3mm.
DisplayPort AUX CH intra-pair matching should be 0.127mm. Max length 330.2mm.
Max length of LVDS/DisplayPort/TMDS traces: 13 inches.
SOURCE: Calpella SFF DG Rev 1.5 (407364) and Family GPU DG-04202-001-v04.

GDDR5 FB A Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
FB_A0_CLK	GDDR5_80D	GDDR5_CLK	FB A0 CLK P	75 76
FB_A0_CLK	GDDR5_80D	GDDR5_CLK	FB A0 CLK N	75 76
FB_A1_CLK	GDDR5_80D	GDDR5_CLK	FB A1 CLK P	75 76
FB_A1_CLK	GDDR5_80D	GDDR5_CLK	FB A1 CLK N	75 76
FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB A0 A<8..0>	6 75 76
FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB A1 A<8..0>	6 75 76
FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB A0 ABI L	6 75 76
FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB A1 ABI L	6 75 76
FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB A0 RAS L	75 76
FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB A1 RAS L	75 76
FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB A0 CAS L	75 76
FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB A1 CAS L	75 76
FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB A0 WE L	75 76
FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB A1 WE L	75 76
FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB A0 CKE L	75 76
FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB A1 CKE L	75 76
FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB A0 CS L	75 76
FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB A1 CS L	75 76
FB_A0_EDC0	GDDR5_45SE	GDDR5_EDC	FB A0 EDC<0>	6 75 76
FB_A0_EDC1	GDDR5_45SE	GDDR5_EDC	FB A0 EDC<1>	6 75 76
FB_A0_EDC2	GDDR5_45SE	GDDR5_EDC	FB A0 EDC<2>	6 75 76
FB_A0_EDC3	GDDR5_45SE	GDDR5_EDC	FB A0 EDC<3>	6 75 76
FB_A1_EDC0	GDDR5_45SE	GDDR5_EDC	FB A1 EDC<0>	6 75 76
FB_A1_EDC1	GDDR5_45SE	GDDR5_EDC	FB A1 EDC<1>	6 75 76
FB_A1_EDC2	GDDR5_45SE	GDDR5_EDC	FB A1 EDC<2>	6 75 76
FB_A1_EDC3	GDDR5_45SE	GDDR5_EDC	FB A1 EDC<3>	6 75 76
FB_A0_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB A0 DBI L<0>	6 75 76
FB_A0_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB A0 DBI L<1>	6 75 76
FB_A0_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB A0 DBI L<2>	6 75 76
FB_A0_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB A0 DBI L<3>	6 75 76
FB_A1_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB A1 DBI L<0>	6 75 76
FB_A1_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB A1 DBI L<1>	6 75 76
FB_A1_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB A1 DBI L<2>	6 75 76
FB_A1_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB A1 DBI L<3>	6 75 76
FB_A0_WCLK0	GDDR5_80D	GDDR5_CMD	FB A0 WCLK P<0>	6 75 76
FB_A0_WCLK0	GDDR5_80D	GDDR5_CMD	FB A0 WCLK N<0>	6 75 76
FB_A0_WCLK1	GDDR5_80D	GDDR5_CMD	FB A0 WCLK P<1>	6 75 76
FB_A0_WCLK1	GDDR5_80D	GDDR5_CMD	FB A0 WCLK N<1>	6 75 76
FB_A1_WCLK0	GDDR5_80D	GDDR5_CMD	FB A1 WCLK P<0>	6 75 76
FB_A1_WCLK0	GDDR5_80D	GDDR5_CMD	FB A1 WCLK N<0>	6 75 76
FB_A1_WCLK1	GDDR5_80D	GDDR5_CMD	FB A1 WCLK P<1>	6 75 76
FB_A1_WCLK1	GDDR5_80D	GDDR5_CMD	FB A1 WCLK N<1>	6 75 76
FB_A0_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB A0 DQ<7..0>	6 75 76
FB_A0_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB A0 DQ<15..8>	6 75 76
FB_A0_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB A0 DQ<23..16>	6 75 76
FB_A0_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB A0 DQ<31..24>	6 75 76
FB_A1_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB A1 DQ<7..0>	6 75 76
FB_A1_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB A1 DQ<15..8>	6 75 76
FB_A1_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB A1 DQ<23..16>	6 75 76
FB_A1_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB A1 DQ<31..24>	6 75 76
FB_AB_RESET	GDDR5_45R50SE	GDDR5_CMD	FB RESET L	75 76 77

GDDR5 FB B Net Properties


ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
FB_B0_CLK	GDDR5_80D	GDDR5_CLK	FB B0 CLK P	75 77
FB_B0_CLK	GDDR5_80D	GDDR5_CLK	FB B0 CLK N	75 77
FB_B1_CLK	GDDR5_80D	GDDR5_CLK	FB B1 CLK P	75 77
FB_B1_CLK	GDDR5_80D	GDDR5_CLK	FB B1 CLK N	75 77
FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB B0 A<8..0>	6 75 77
FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB B1 A<8..0>	6 75 77
FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB B0 ABI L	6 75 77
FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB B1 ABI L	6 75 77
FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB B0 RAS L	75 77
FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB B1 RAS L	75 77
FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB B0 CAS L	75 77
FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB B1 CAS L	75 77
FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB B0 WE L	75 77
FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB B1 WE L	75 77
FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB B0 CKE L	75 77
FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB B1 CKE L	75 77
FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB B0 CS L	75 77
FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB B1 CS L	75 77
FB_B0_EDC0	GDDR5_45SE	GDDR5_EDC	FB B0 EDC<0>	6 75 77
FB_B0_EDC1	GDDR5_45SE	GDDR5_EDC	FB B0 EDC<1>	6 75 77
FB_B0_EDC2	GDDR5_45SE	GDDR5_EDC	FB B0 EDC<2>	6 75 77
FB_B0_EDC3	GDDR5_45SE	GDDR5_EDC	FB B0 EDC<3>	6 75 77
FB_B1_EDC0	GDDR5_45SE	GDDR5_EDC	FB B1 EDC<0>	6 75 77
FB_B1_EDC1	GDDR5_45SE	GDDR5_EDC	FB B1 EDC<1>	6 75 77
FB_B1_EDC2	GDDR5_45SE	GDDR5_EDC	FB B1 EDC<2>	6 75 77
FB_B1_EDC3	GDDR5_45SE	GDDR5_EDC	FB B1 EDC<3>	6 75 77
FB_B0_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB B0 DBI L<0>	6 75 77
FB_B0_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB B0 DBI L<1>	6 75 77
FB_B0_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB B0 DBI L<2>	6 75 77
FB_B0_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB B0 DBI L<3>	6 75 77
FB_B1_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB B1 DBI L<0>	6 75 77
FB_B1_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB B1 DBI L<1>	6 75 77
FB_B1_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB B1 DBI L<2>	6 75 77
FB_B1_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB B1 DBI L<3>	6 75 77
FB_B0_WCLK0	GDDR5_80D	GDDR5_CMD	FB B0 WCLK P<0>	6 75 77
FB_B0_WCLK0	GDDR5_80D	GDDR5_CMD	FB B0 WCLK N<0>	6 75 77
FB_B0_WCLK1	GDDR5_80D	GDDR5_CMD	FB B0 WCLK P<1>	6 75 77
FB_B0_WCLK1	GDDR5_80D	GDDR5_CMD	FB B0 WCLK N<1>	6 75 77
FB_B1_WCLK0	GDDR5_80D	GDDR5_CMD	FB B1 WCLK P<0>	6 75 77
FB_B1_WCLK0	GDDR5_80D	GDDR5_CMD	FB B1 WCLK N<0>	6 75 77
FB_B1_WCLK1	GDDR5_80D	GDDR5_CMD	FB B1 WCLK P<1>	6 75 77
FB_B1_WCLK1	GDDR5_80D	GDDR5_CMD	FB B1 WCLK N<1>	6 75 77
FB_B0_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB B0 DQ<7..0>	6 75 77
FB_B0_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB B0 DQ<15..8>	6 75 77
FB_B0_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB B0 DQ<23..16>	6 75 77
FB_B0_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB B0 DQ<31..24>	6 75 77
FB_B1_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB B1 DQ<7..0>	6 75 77
FB_B1_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB B1 DQ<15..8>	6 75 77
FB_B1_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB B1 DQ<23..16>	6 75 77
FB_B1_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB B1 DQ<31..24>	6 75 77

MUXGFX Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
LVDS_A_CLK	LVDS_85D	LVDS	LVDS A CLK P	83 87
LVDS_A_CLK	LVDS_85D	LVDS	LVDS A CLK N	83 87
LVDS_A_DATA	LVDS_85D	LVDS	LVDS A DATA P<2..0>	83 87
LVDS_A_DATA	LVDS_85D	LVDS	LVDS A DATA N<2..0>	83 87
LVDS_B_CLK	LVDS_85D	LVDS	LVDS B CLK P	83 87
LVDS_B_CLK	LVDS_85D	LVDS	LVDS B CLK N	83 87
LVDS_B_DATA	LVDS_85D	LVDS	LVDS B DATA P<2..0>	83 87
LVDS_B_DATA	LVDS_85D	LVDS	LVDS B DATA N<2..0>	83 87
	LVDS_85D	LVDS	LVDS CONN A CLK F P	6 82
	LVDS_85D	LVDS	LVDS CONN A CLK F N	6 82
	LVDS_85D	LVDS	LVDS CONN B CLK F P	6 82
	LVDS_85D	LVDS	LVDS CONN B CLK F N	6 82
	LVDS_85D	LVDS	LVDS CONN A CLK P	82 83
	LVDS_85D	LVDS	LVDS CONN A CLK N	82 83
	LVDS_85D	LVDS	LVDS CONN A DATA P<2..0>	6 82 83
	LVDS_85D	LVDS	LVDS CONN A DATA N<2..0>	6 82 83
	LVDS_85D	LVDS	LVDS CONN B CLK P	82 83
	LVDS_85D	LVDS	LVDS CONN B CLK N	82 83
	LVDS_85D	LVDS	LVDS CONN B DATA P<2..0>	6 82 83
	LVDS_85D	LVDS	LVDS CONN B DATA N<2..0>	6 82 83

Whistler Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
GPU_CLK27M	CLK_SLOW_55S	CLK_SLOW	GPU CLK27M	78 79
GPU_CLK100M	CLK_SLOW_55S	CLK_SLOW	GPU CLK100M	78 79
LVDS_EG_A_CLK	LVDS_85D	LVDS	LVDS EG A CLK P	78 87
LVDS_EG_A_CLK	LVDS_85D	LVDS	LVDS EG A CLK N	78 87
LVDS_EG_A_DATA	LVDS_85D	LVDS	LVDS EG A DATA P<2..0>	78 87
LVDS_EG_A_DATA	LVDS_85D	LVDS	LVDS EG A DATA N<2..0>	78 87
LVDS_EG_A_DATA3	LVDS_85D	LVDS	NC LVDS EG A DATA P<3>	78 79
LVDS_EG_A_DATA3	LVDS_85D	LVDS	NC LVDS EG A DATA N<3>	78 79
LVDS_EG_B_DATA	LVDS_85D	LVDS	LVDS EG B DATA P<2..0>	78 87
LVDS_EG_B_DATA	LVDS_85D	LVDS	LVDS EG B DATA N<2..0>	78 87
LVDS_EG_B_DATA3	LVDS_85D	LVDS	NC LVDS EG B DATA P<3>	78 79
LVDS_EG_B_DATA3	LVDS_85D	LVDS	NC LVDS EG B DATA N<3>	78 79
DP_ML	DP_85D	DISPLAYPORT	DP EXTA ML C P<3..0>	78 84
DP_85D	DP_85D	DISPLAYPORT	DP EXTA ML C N<3..0>	78 84
DP_AUX_CH	DP_85D	DISPLAYPORT	DP EXTA AUXCH C P	83 84
DP_AUX_CH	DP_85D	DISPLAYPORT	DP EXTA AUXCH C N	83 84
DP_AUX_CH	DP_85D	DISPLAYPORT	DP EG AUXCH P	6 78 83
DP_AUX_CH	DP_85D	DISPLAYPORT	DP EG AUXCH N	6 78 83

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GPU (Whistler) CONSTRAINTS			
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NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS_85D	BGA	LVDS_85D
DP_85D	BGA	100_DIFF_BGA
SATA_90D	BGA	100_DIFF_BGA
CLK_PCIE_90D	BGA	100_DIFF_BGA

Allow 0.127 mm necks for >0.127 mm lines for ARD fanout.


PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_72D	BOTTOM			0.127 MM	6.35 MM		
MEM_85D	TOP			0.1 MM	6.35 MM		

5

899	AUDIO DIFFPAIR	AUDIOIFF	AUDIO	AUD LO1 R P	59
900		AUDIOIFF	AUDIO	AUD LO1 R N	59
910	AUDIO DIFFPAIR	AUDIOIFF	AUDIO	AUD LO2 L P	59
911		AUDIOIFF	AUDIO	AUD LO2 L N	59
920	AUDIO DIFFPAIR	AUDIOIFF	AUDIO	AUD LO2 R P	59
921		AUDIOIFF	AUDIO	AUD LO2 R N	59
930	AUDIO DIFFPAIR	AUDIOIFF	AUDIO	AUD SPKRAMP LIN P	59
931		AUDIOIFF	AUDIO	AUD SPKRAMP LIN N	59
940	AUDIO DIFFPAIR	AUDIOIFF	AUDIO	AUD SPKRAMP RIN P	59
941		AUDIOIFF	AUDIO	AUD SPKRAMP RIN N	59
950	AUDIO DIFFPAIR	AUDIOIFF	AUDIO	AUD SPKRAMP SUBIN P	59
951		AUDIOIFF	AUDIO	AUD SPKRAMP SUBIN N	59

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ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING
PCIE CLK100M AP	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M AP CONN P 6 31
	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M AP CONN N 6 31
	1T01_DIEFFPAIR		CHGR CSI R P 63
	1T01_DIEFFPAIR		CHGR CSI R N 63
	1T01_DIEFFPAIR		CHGR CSO R P 49 63
	1T01_DIEFFPAIR		CHGR CSO R N 49 63
(USB_EXTA)	USB_R5D	USB	USB2 EXTA MUXED P 42
(USB_EXTA)	USB_R5D	USB	USB2 EXTA MUXED N 42
(USB_EXTA)	USB_R5D	USB	USB2 LT1 P 6 42
(USB_EXTA)	USB_R5D	USB	USB2 LT1 N 6 42
	USB_R5D	USB	CONN USB2_BT P 6
	USB_R5D	USB	CONN USB2_BT N 6
	USB_R5D	USB	USB LT2 P 6 42
	USB_R5D	USB	USB LT2 N 6 42
SSM2375L	AUDIO_DIEFFPAIR	AUDIO	SSM2375L P 59
SSM2375L	AUDIO_DIEFFPAIR	AUDIO	SSM2375L N 59
SSM2375R	AUDIO_DIEFFPAIR	AUDIO	SSM2375R P 59
SSM2375R	AUDIO_DIEFFPAIR	AUDIO	SSM2375R N 59
SSM2375S	AUDIO_DIEFFPAIR	AUDIO	SSM2375S P 59
SSM2375S	AUDIO_DIEFFPAIR	AUDIO	SSM2375S N 59
SPK_OUT	DIEFFPAIR	AUDIO	SPKRCONN L OUT P 6 59 60
	DIEFFPAIR	AUDIO	SPKRCONN L OUT N 6 59 60
SPK_OUT	DIEFFPAIR	AUDIO	SPKRCONN R OUT P 6 59 60
	DIEFFPAIR	AUDIO	SPKRCONN R OUT N 6 59 60
SPK_OUT	DIEFFPAIR	AUDIO	SPKRCONN S OUT P 6 59 60
	DIEFFPAIR	AUDIO	SPKRCONN S OUT N 6 59 60
	USB_R5D	USB	USB TPAD R P 62
	USB_R5D	USB	USB TPAD R N 62
		SR_POWER	PP3V3 S5 45 56 65 70 71 72 82 85 89
		SR_POWER	PP3V3 S0 48 49 50 51 53 56 60 61 71 73
		SR_POWER	PP1V5 S3RS0 76 23 33 34 35 36 39 40 41 45 47
		GND	GND 6

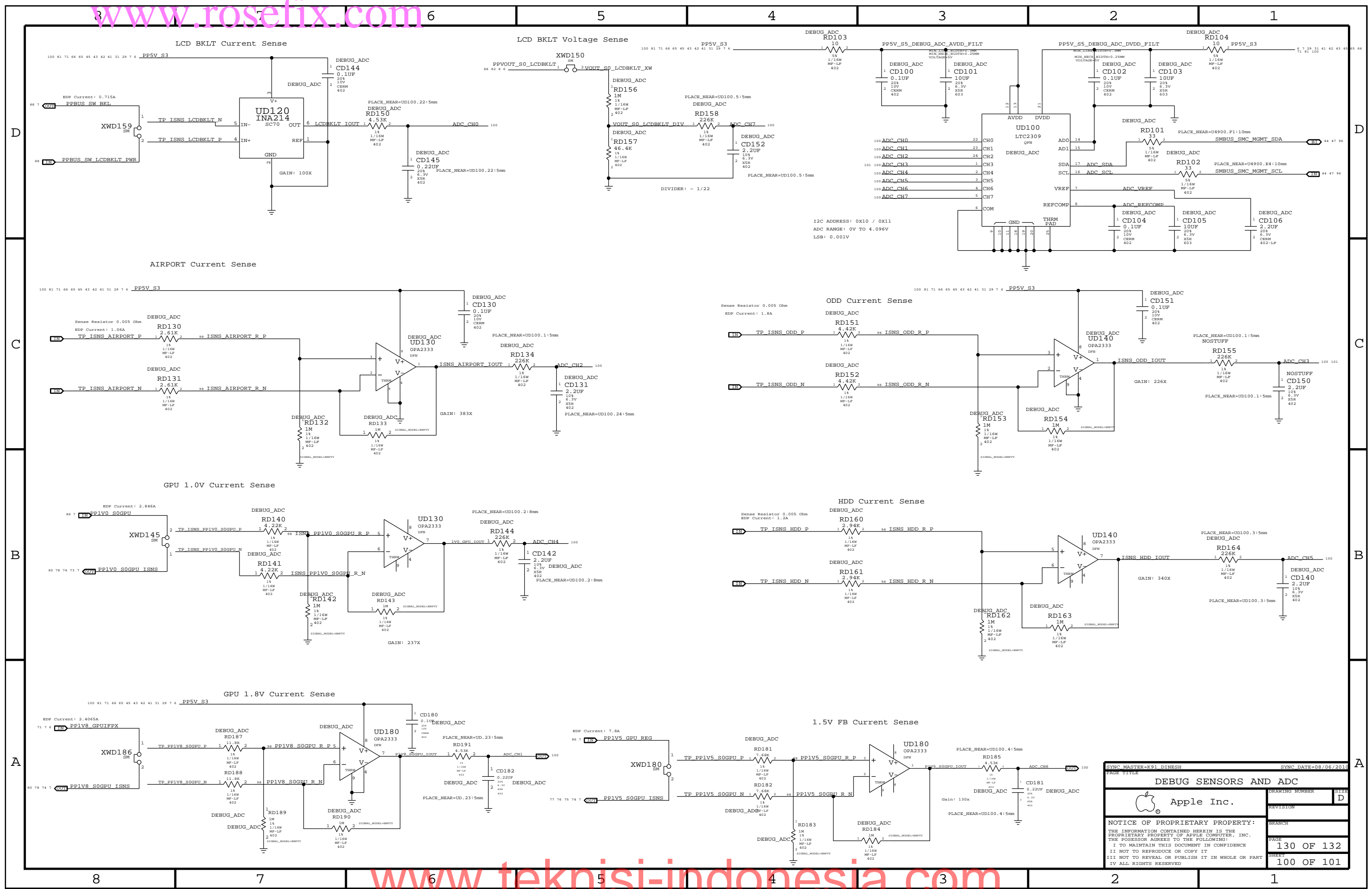
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